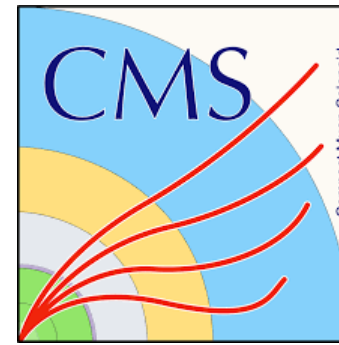


한국고에너지물리학회 2025 가을 총회
한국물리학회 핵 입자 천체물리학분과 합동 워크숍

2025년 11월 19일 (수) - 22일 (토)
전남대학교



Korea's Contributions to the CMS Endcap Timing Layer for the HL-LHC Upgrade

CHANG-SEONG MOON

Representative of Korea CMS team

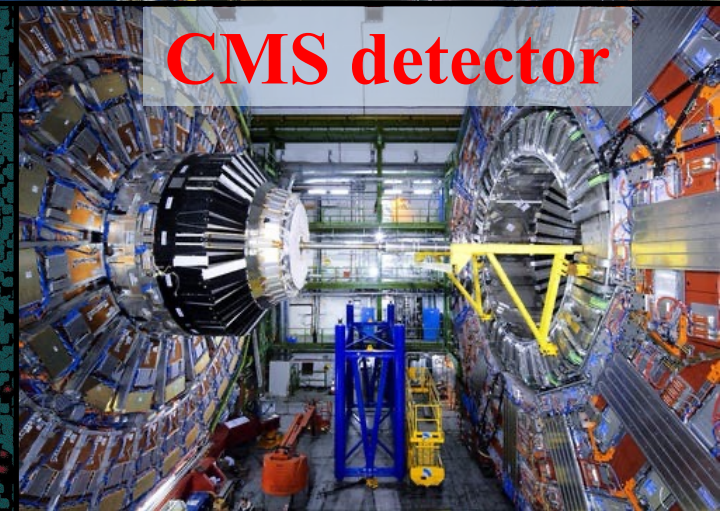
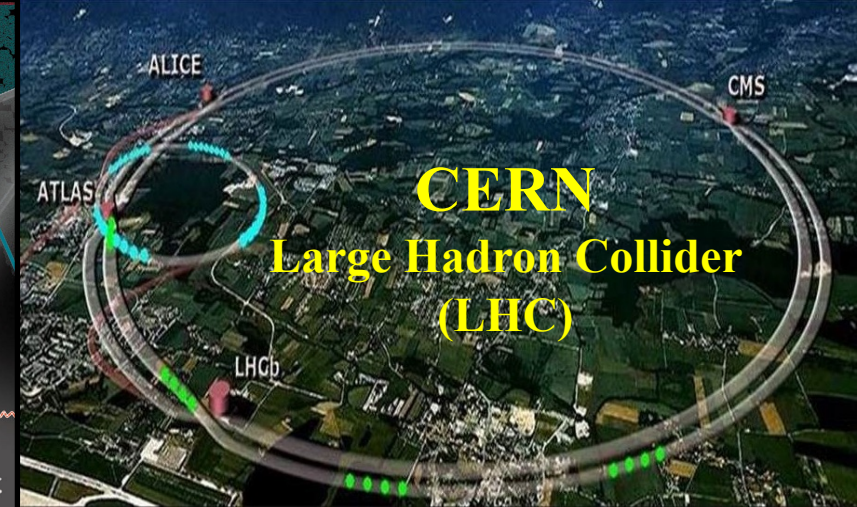
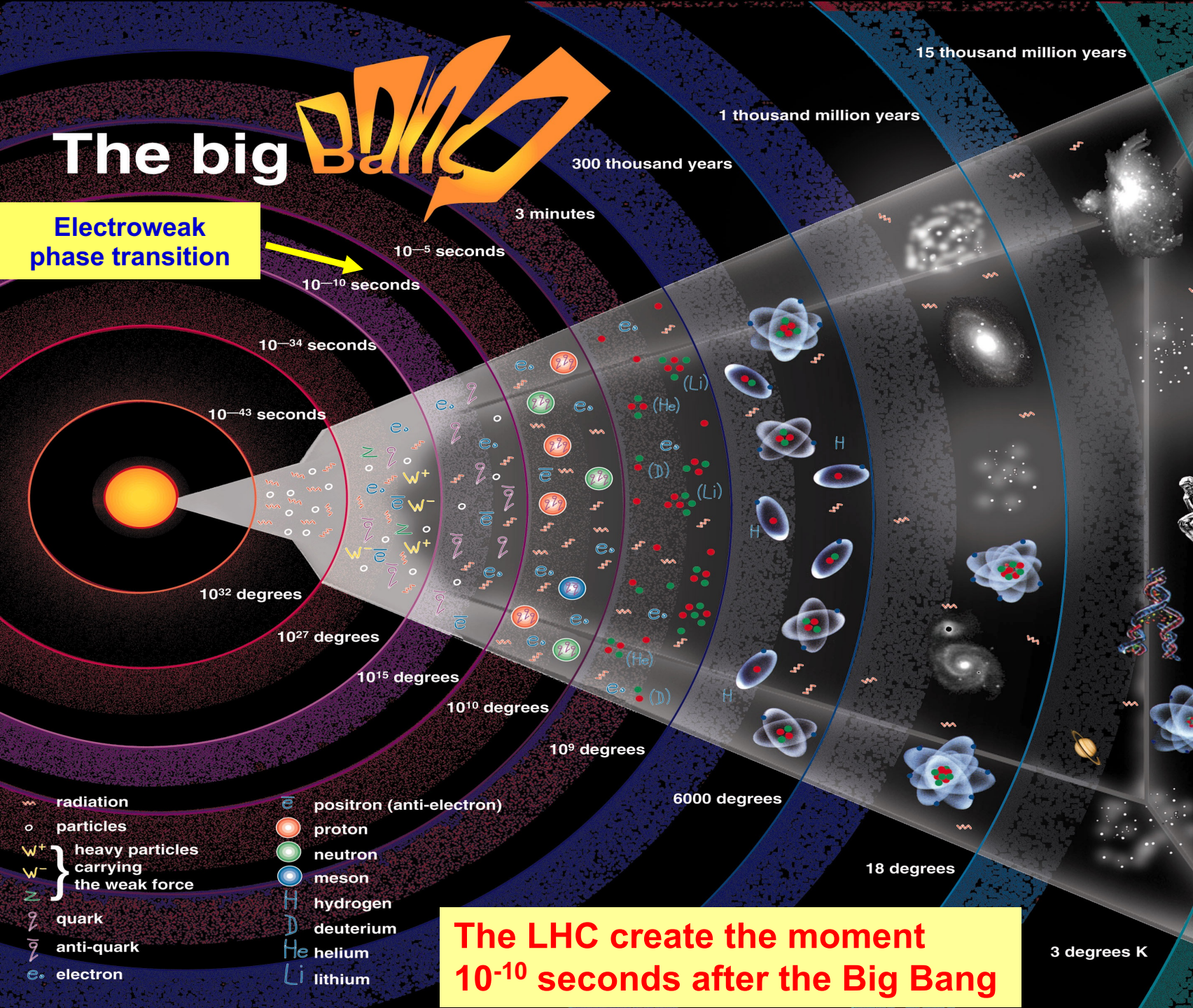
Centre for High Energy Physics (CHEP), Kyungpook National University (KNU)

한국고에너지물리학회 및 핵-입자-천체분과 연합 워크숍, Nov. 20 2025

The big Bang



Electroweak
phase transition



The LHC create the moment
 10^{-10} seconds after the Big Bang

High-Luminosity LHC (HL-LHC) at CERN

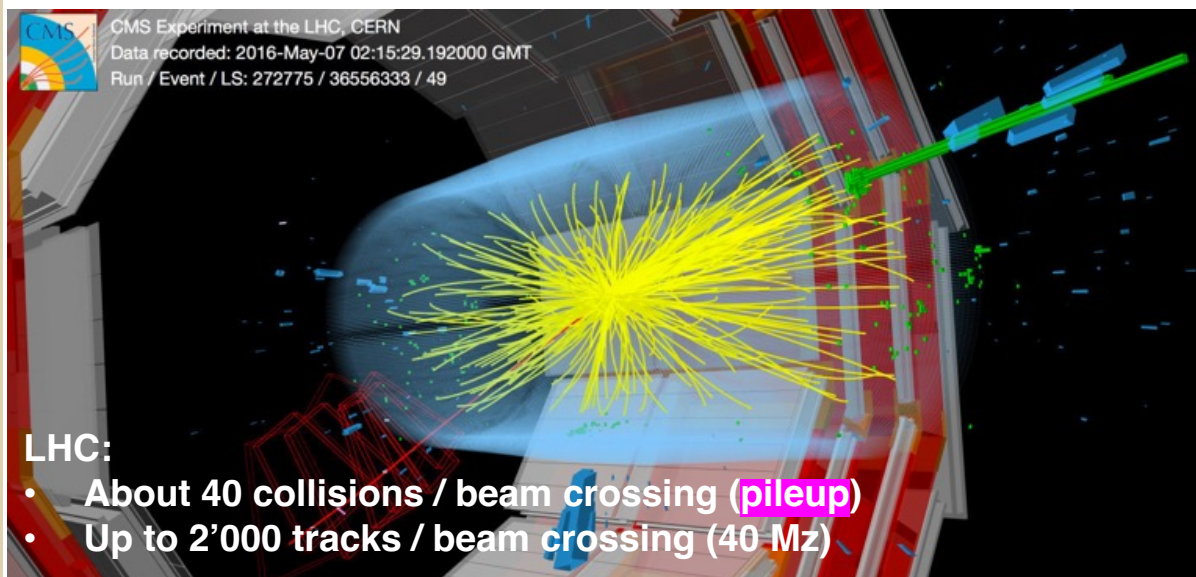
Goal: precision tests of the standard model and Higgs physics, and searches for (rare) BSM phenomena

- ❑ Precision measurement of Higgs boson couplings (few percent)
- ❑ Measurement of the **Higgs boson self-coupling** via direct observation of the di-Higgs boson production
- ❑ Search for heavy **dark matter** candidates, **SUSY** particles, new gauge bosons, **Long-Lived Particles**, ...

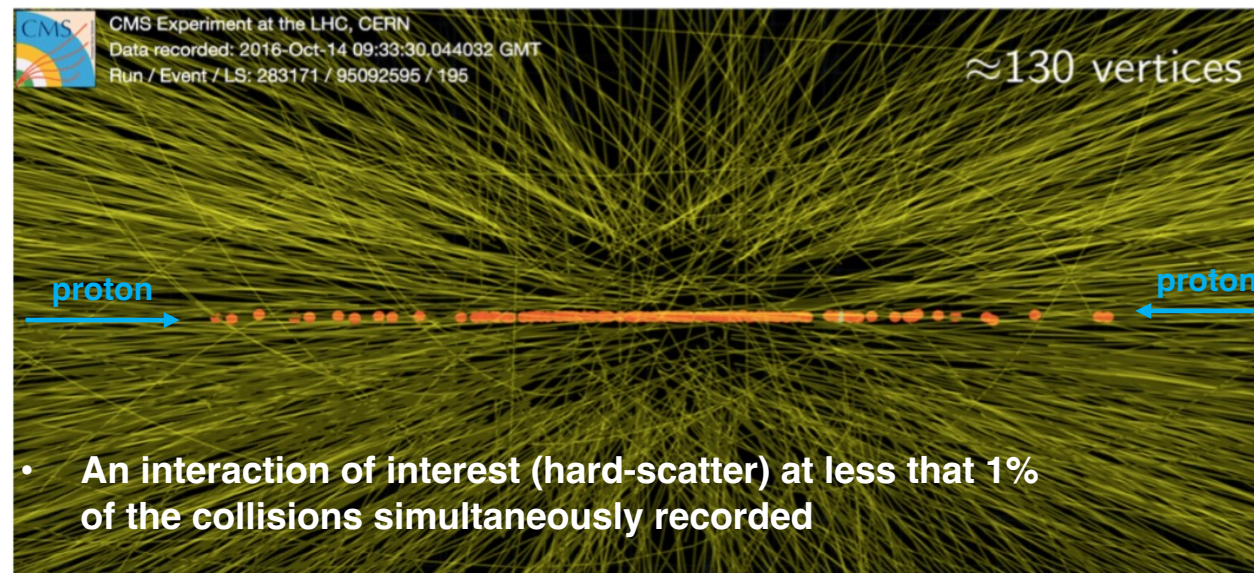
Means: upgrade of the LHC optics and injectors to increase the beam intensity

- ❑ Luminosity delivered by **LHC** (2009-2026): $\sim 400 \text{ fb}^{-1}$ / experiment [$\sim 250 \text{ fb}^{-1}$ collected so far]
- ❑ Target luminosity for **HL-LHC** (2030-2042): $> 3000 \text{ fb}^{-1}$ / experiment [*one year of HL-LHC equivalent to ~ 10 years of LHC*]

Collision event with 35 reconstructed vertices

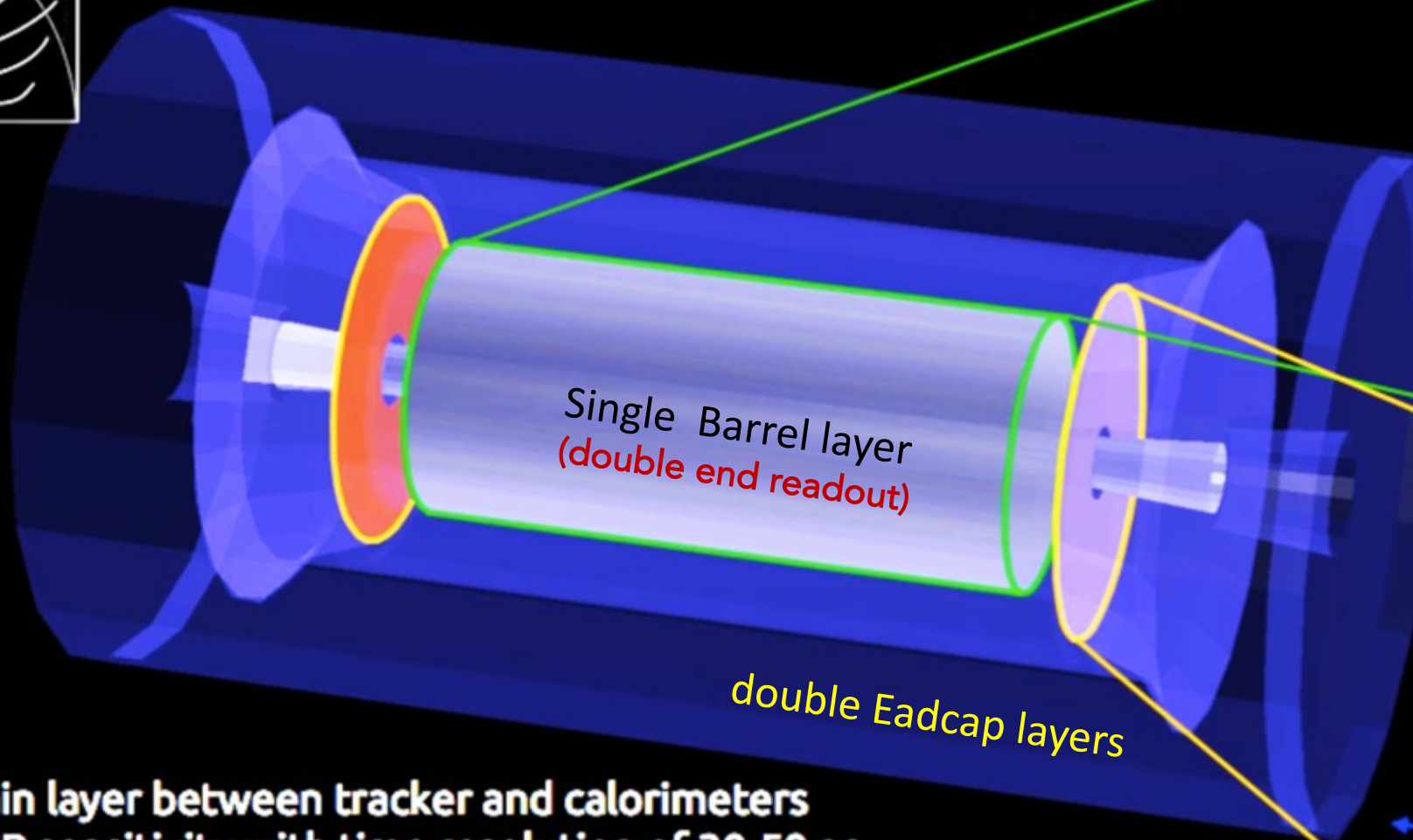


Real life event at the LHC emulating HL-LHC conditions



- ❑ Important to maintain detector performance during HL-LHC running
 - Time information will help to reduce pileup effects from approximately 200 simultaneous interactions
- ❑ MIP timing detector (MTD) consists of barrel timing layer (BTL) and endcap timing layer (ETL), providing 30-50 ps time resolution per track
 - BTL: LYSO crystal scintillator + SiPM readout
 - ETL: Silicon based sensor (LGAD) + ASIC readout
 - Two different detector technologies for radiation hardness and costs

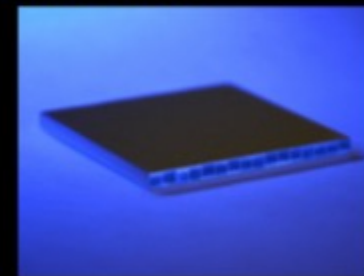
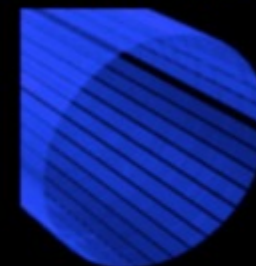
Mip Timing Detector (MTD)



- Thin layer between tracker and calorimeters
- MIP sensitivity with time resolution of 30-50 ps
- Hermetic coverage for $|\eta| < 3.0$

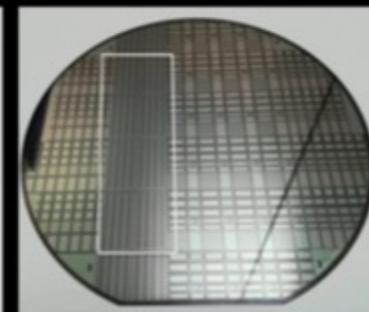
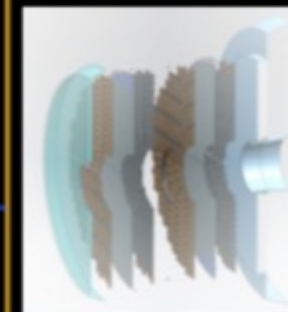
BARREL

Surface $\sim 40 \text{ m}^2$
Number of channels $\sim 332\text{k}$
Radiation level $\sim 2 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$
Sensors: LYSO crystals + SiPMs



ENDCAPS

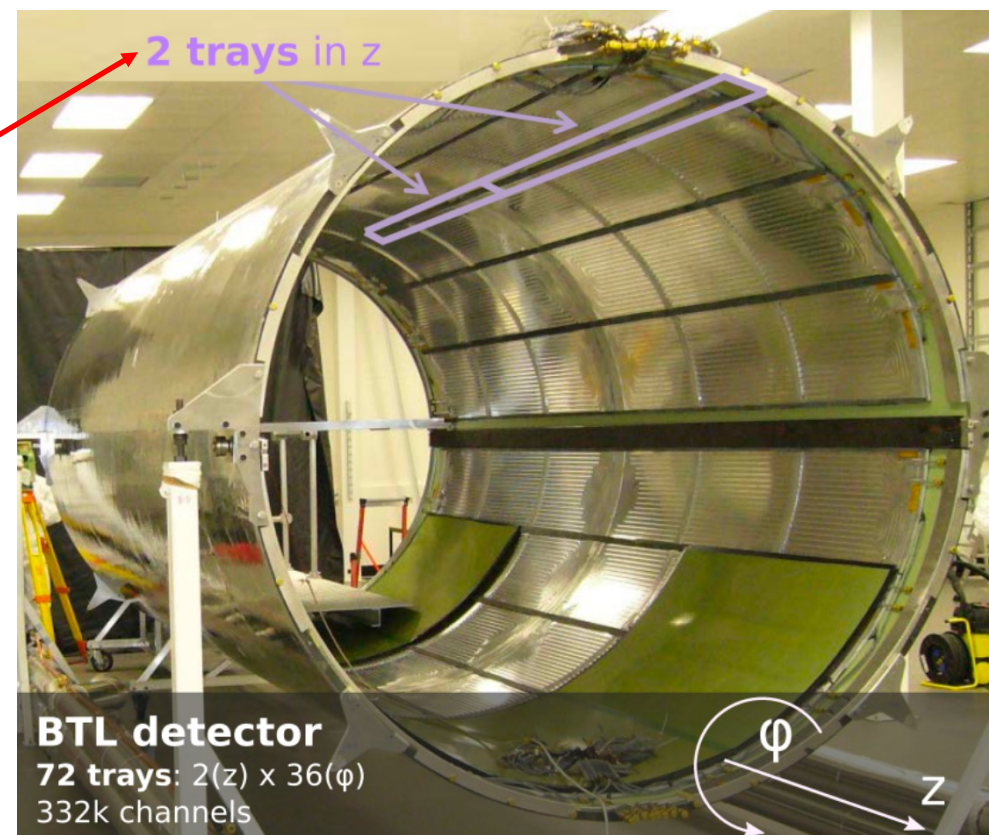
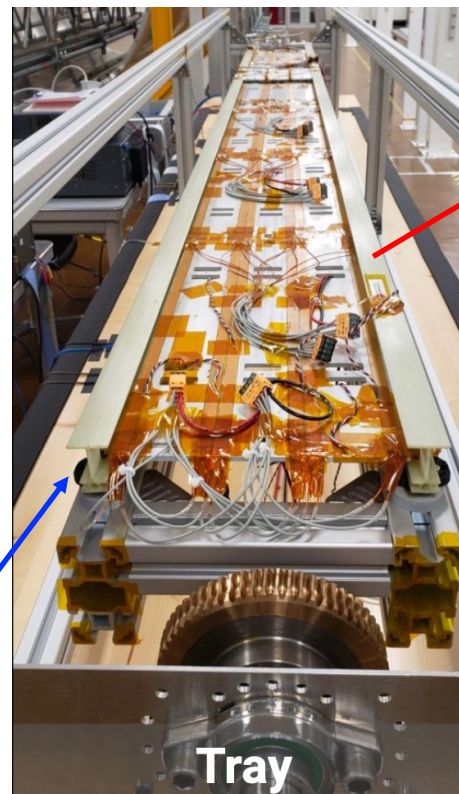
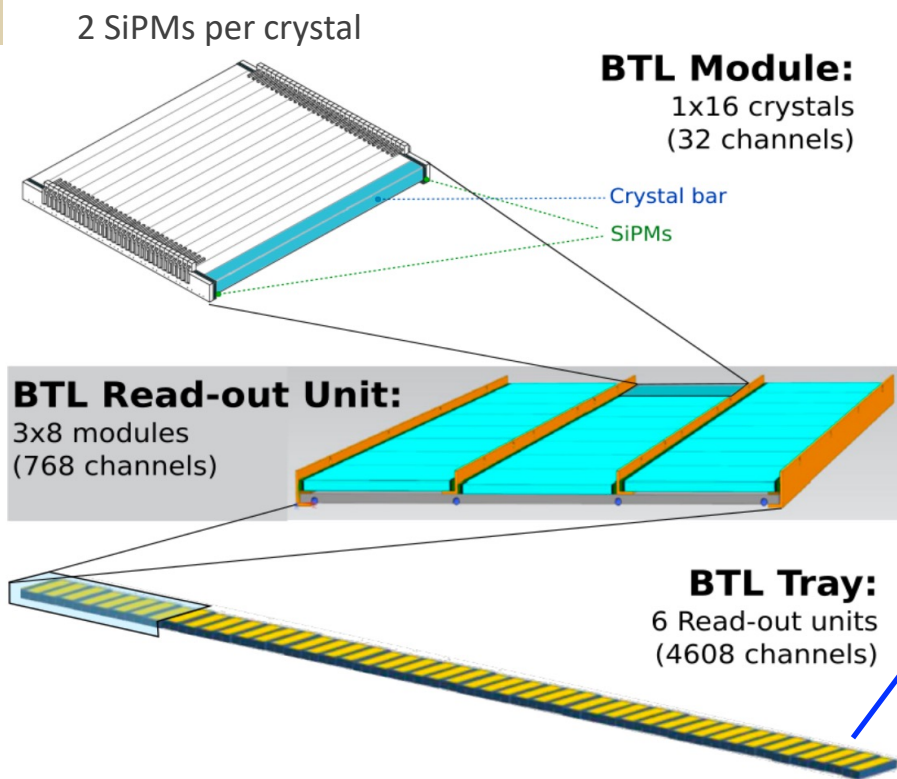
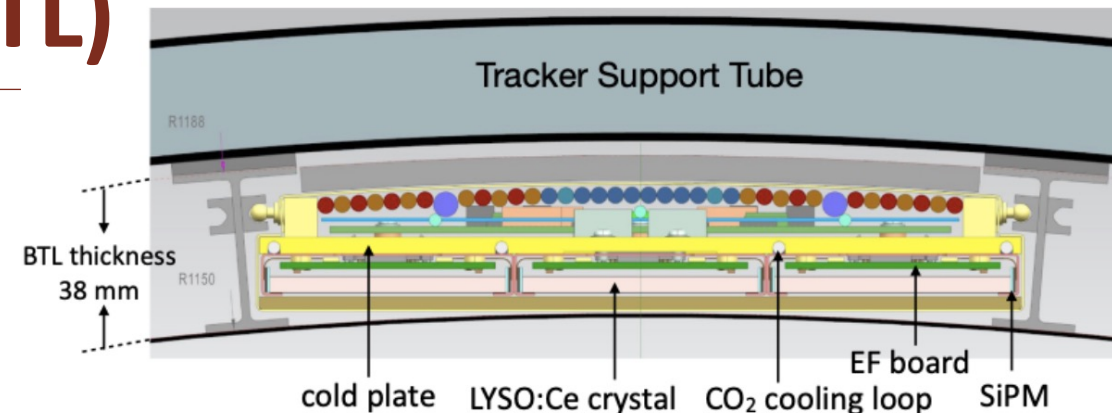
Surface $\sim 14 \text{ m}^2$
Number of channels $\sim 8500 \text{ K}$
Radiation level $\sim 2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
Sensors: Low gain avalanche diodes



Korea's contributions focus exclusively on the ETL project within the CMS MTD upgrade

MTD Barrel Timing Layer (BTL)

- 3.8 cm thin cylindrical detector
 - located inside the tracker support tube, $|\eta| < 1.45$
 - ~ 5 m long, 38 m^2 surface

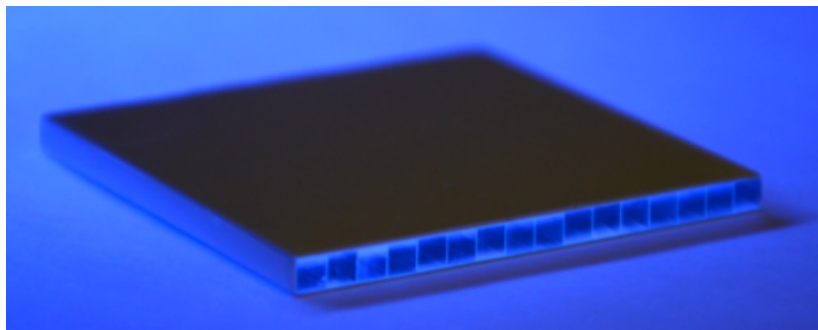
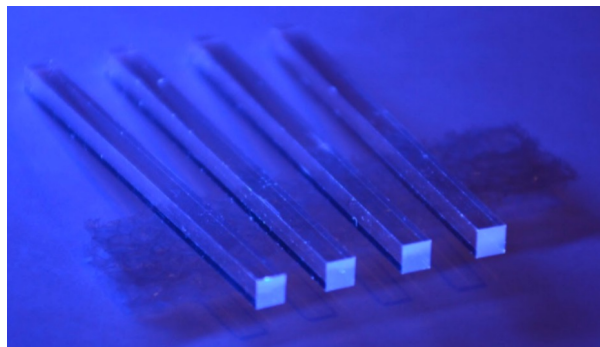


- BTL construction: starting in early 2024!

BTL sensors : LYSO crystal

□ LYSO crystal bars (166k)

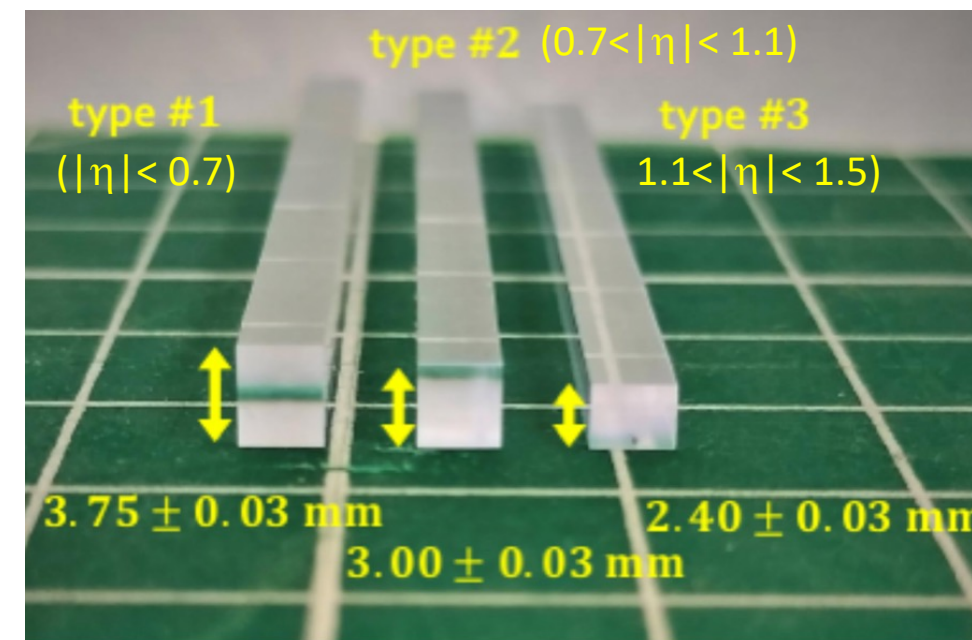
- Cerium-doped lutetium yttrium orthosilicate (LYSO:Ce) scintillation medium
- Well established in PET applications and vendors widely available
- High radiation tolerance
- $\tau_{\text{rise}} : \sim 100 \text{ ps}$, $\tau_{\text{decay}} : \sim 40 \text{ ns}$
- High Light Yield : 40000 γ/MeV



□ LYSO current status

- Single vendor selected
 - Considerably better offer
 - One of best vendor for performance-wise
 - Reliable vendor (large production capacity)
- Pre-production in progress
 - Ordered in March (2% of the total LYSO arrays)
 - QA/QC and construction database ready

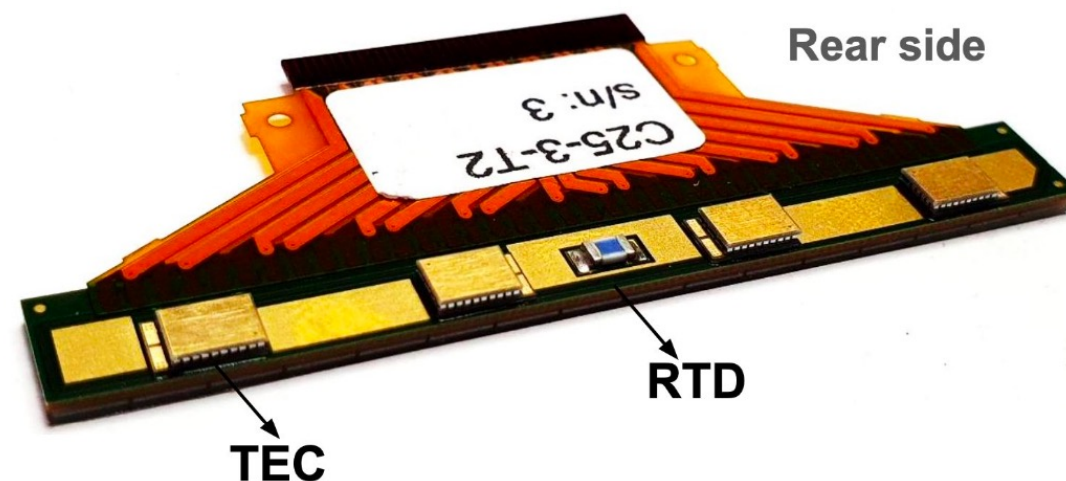
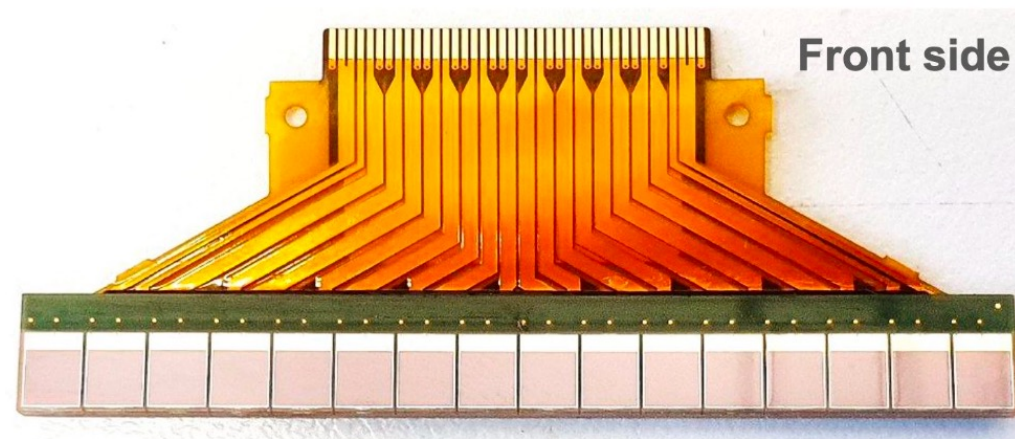
Maximize the crystal light output for 3 η regions



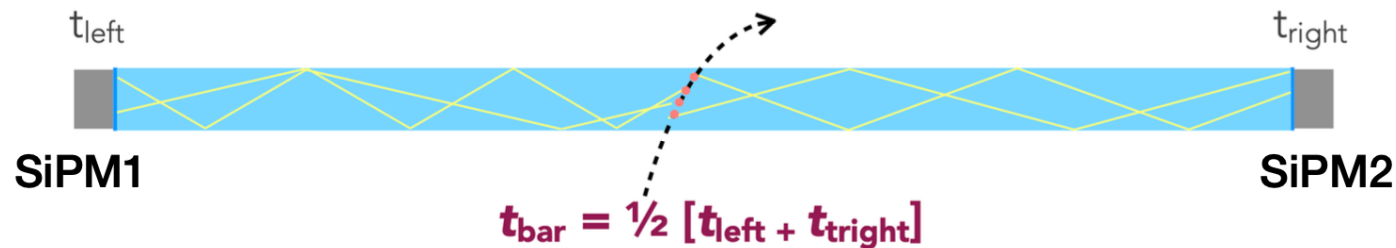
BTL sensors : SiPM

- ❑ SiPM (166k x 2 = 332k channel)
 - Well consolidated technology
 - Photon Detection Efficiency (PDE) : 20–40%
 - Compact, robust, insensitive to magnetic fields
 - Good radiation hardness
 - Fast recovery time <10 ns
 - High dynamic range (10^5)
- ❑ SiPM current status
 - Optimized cell size (25 μm) as a default for BTL
 - Additional performance gain to boost signal
 - SiPM die size ($3.8 \times 2.9 \text{ mm}^2$) fixed to match with the thickest LYSO geometry
- ❑ SiPM plans
 - Tender starts in July
 - Sign the production contract in September
 - First batch delivered ~ Feb. 2024 (for 7 months)

SiPM Module



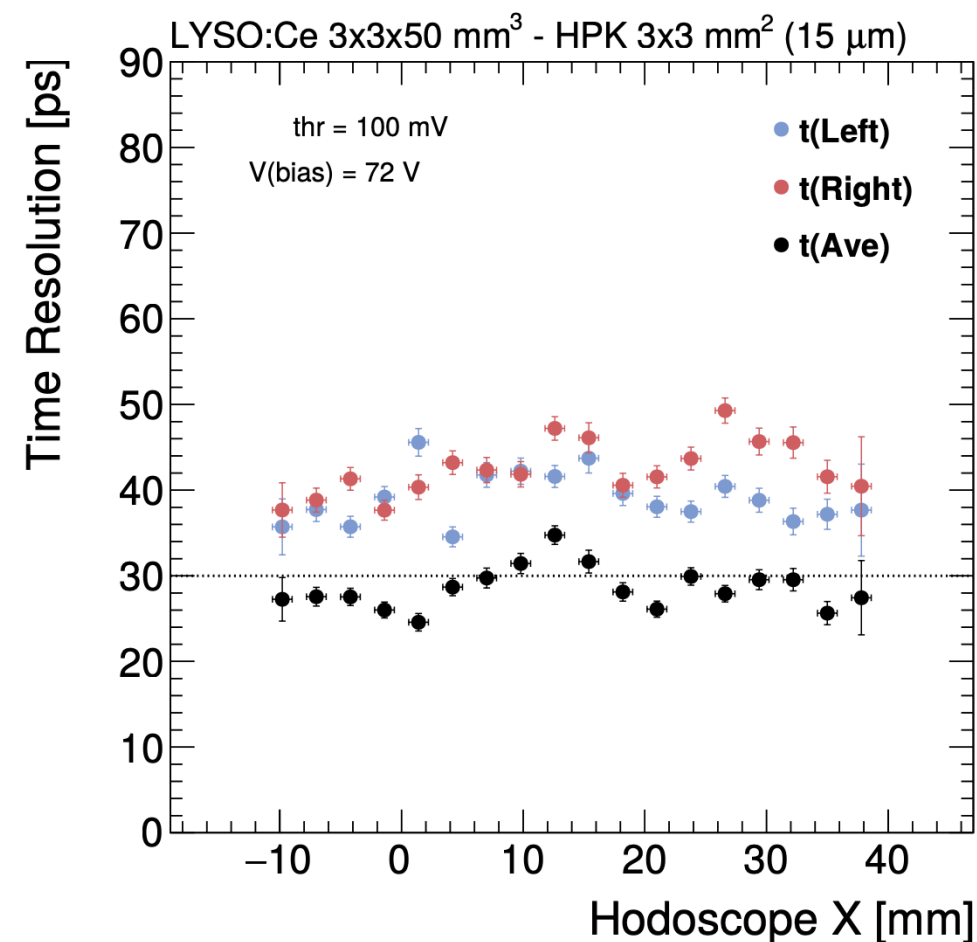
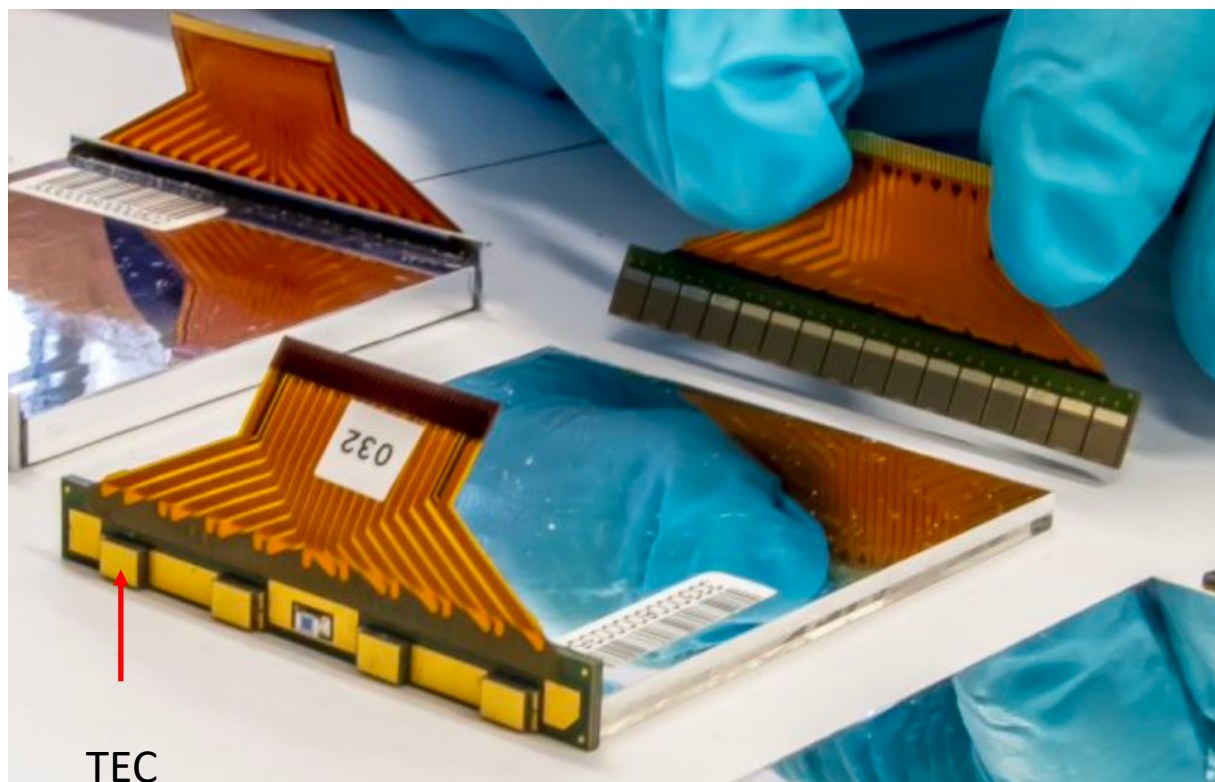
BTL sensors : LYSO crystal and SiPM



LYSO bars with double end readout:

- Improve timing resolution by a factor of $\sqrt{2}$ than single-end

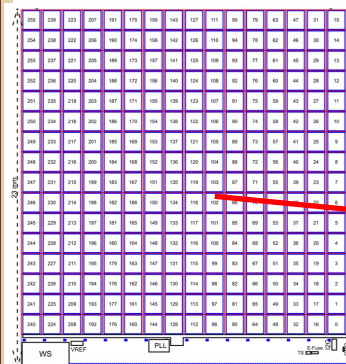
Sensor Module (LYSO + SiPM & TEC)



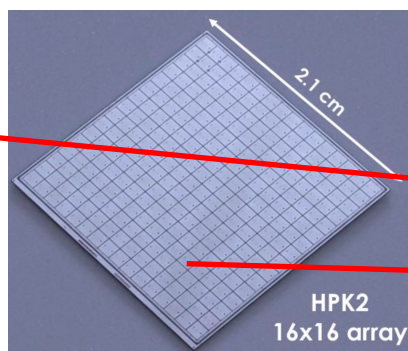
MTD Endcap Timing Layer (ETL)

- ❑ Two double-sided disks for each side
 - Maximize geometrical acceptance (85% per disk)
 - Coverage : $1.6 < |\eta| < 3.0$
 - Average of 1.8 hits per track
 - **Time resolution per track < 35 ps**
 - based on single hit resolution < 50 ps
- ❑ Low-Gain Avalanche Diode (**LGAD**) sensor bump bonded readout ASIC (**ETROC**)

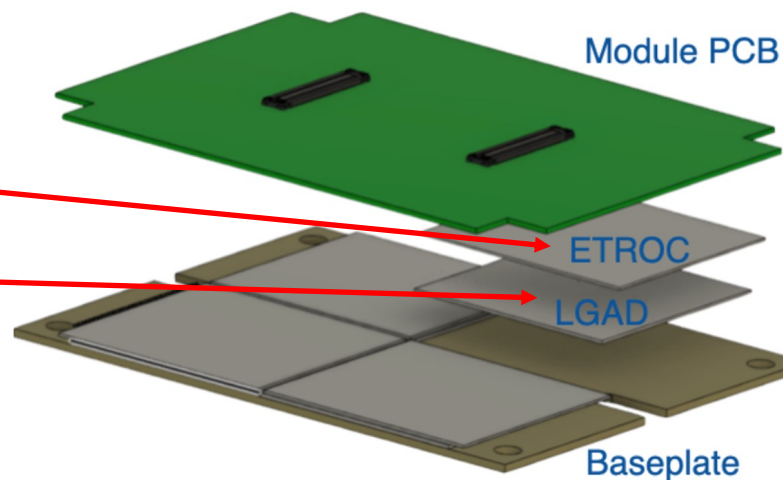
7330 sensors
for each disk (905 kCHF)
→ 123 CHF per sensor



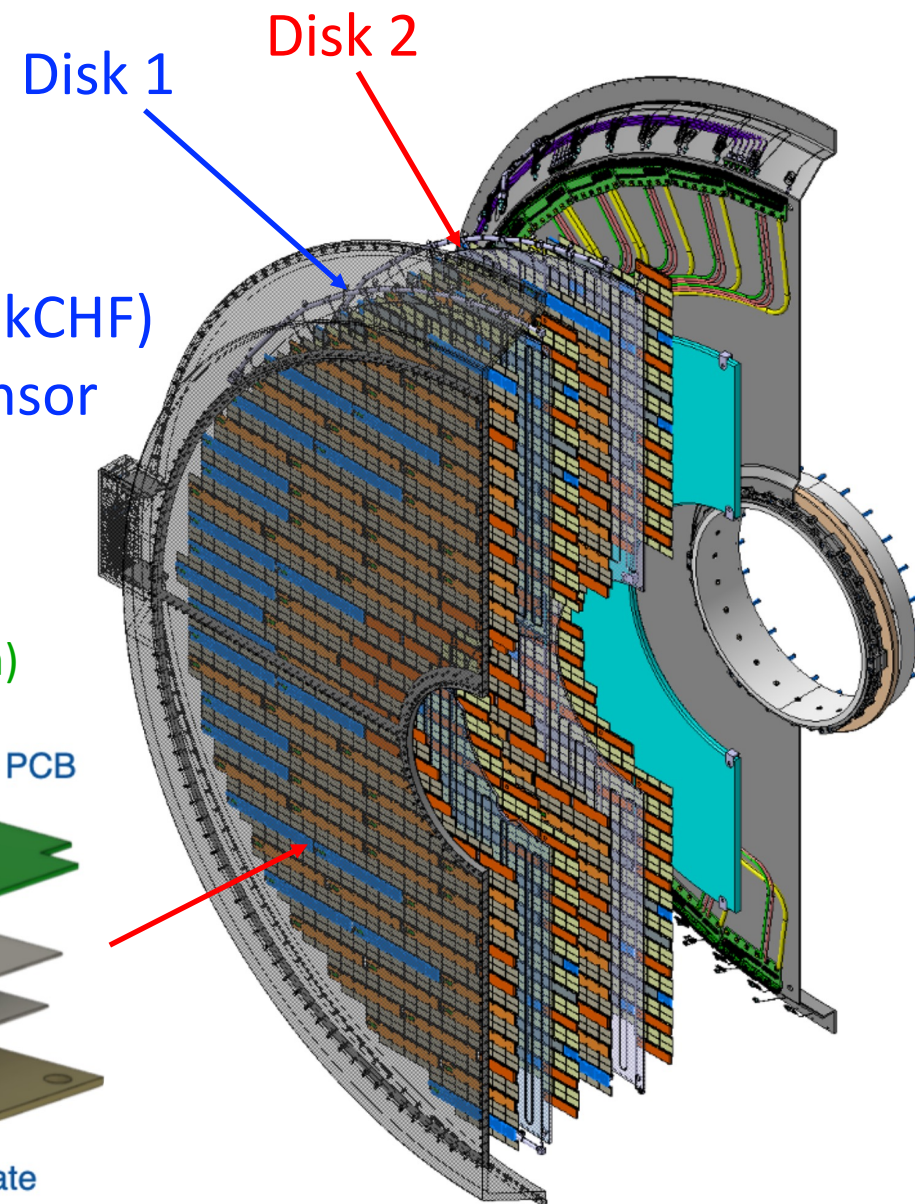
ETROC
(ASIC Chip)



LGAD sensor

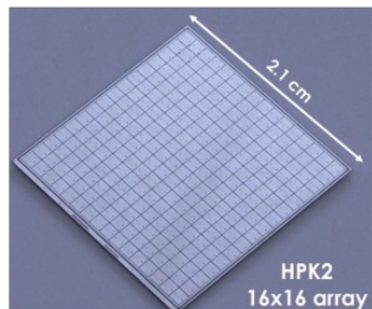


8000 modules (4 sensors each)



31.5 cm < radius < 120 cm

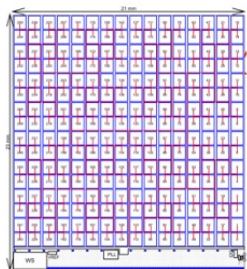
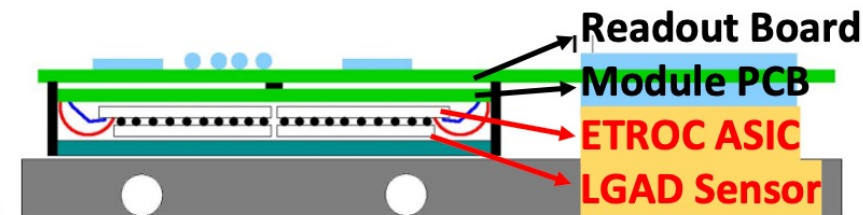
ETL System (1) – LGAD Sensor & ETROC ASIC



Sensor : Low Gain Avalanche Diode **Procurement Phase!**

Silicon-based detector with internal gain layer (Avalanche region)
Achieves fast timing (30~40 ps) with moderate internal gain (10~30)

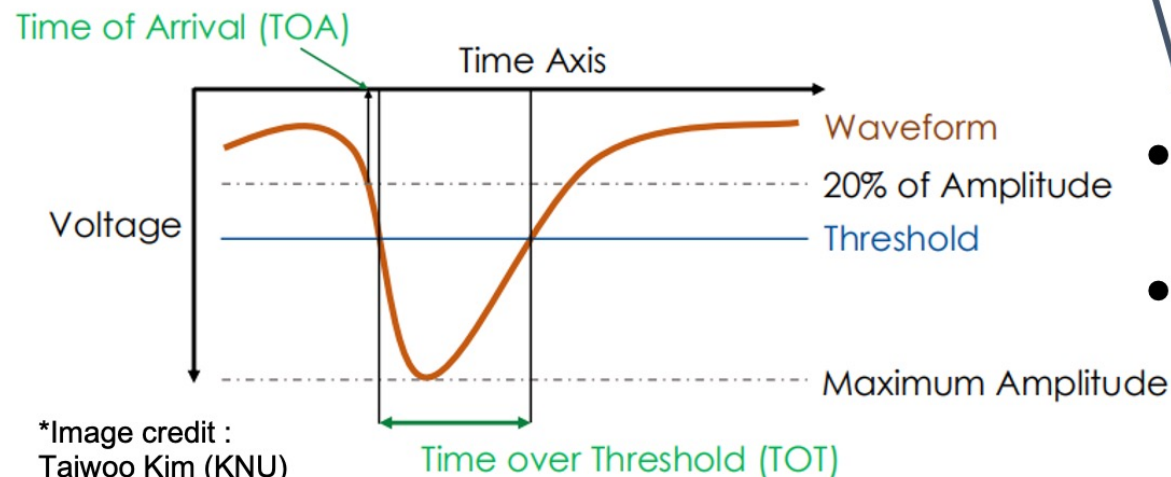
Key challenges: **radiation hardness** ($\sim 2.5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$), and maintaining **Low-noise** under radiation damage
High uniformity and **reliability** in production



ASIC : ETL ReadOut Chip

Readout ASIC bump-bonded directly to LGAD (TSMC 65 nm)
Front-end electronics:

low noise Amplifier, fast Discriminator, and Timing Information



*Image credit :
Taiwoo Kim (KNU)

Sensor and ASIC Procurement Status

- **LGAD Sensor** : Tender (55%) launched in Apr 2025!!
KCMS in-kind contribution of **25% of total LGADs**
Active production/testing ongoing: FBK, L-Foundry (Italy), HPK(Japan) IHEP-IME(China)
USFD-K1/K2 produced at FBK (by KCMS)
- **ETROC2 ASIC** : Test towards PRR* in June 2025!

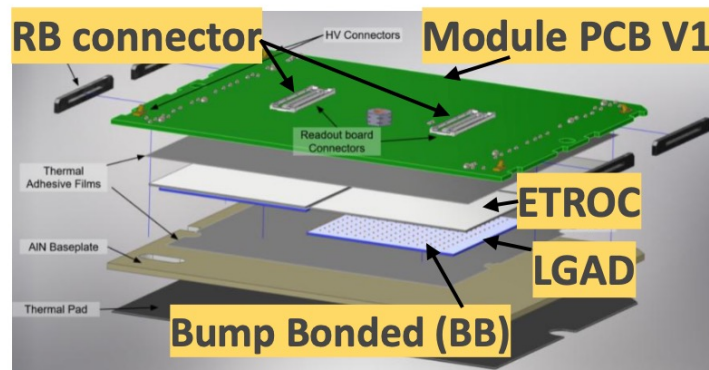


*Procurement Readiness Review

- Precise timing info extraction via **Time to Digital Converter (TDC)**:
Time of Arrival (TOA) and **Time over Threshold (TOT)**
- **Key updates** (2.00 → 2.02/03) : Enhanced digital logic
Global Readout, Calibration, Trigger, Waveform sampler
⇒ **Less noisy** and **Target <40 ps time resolution per hit (system-level)**

ETL System (2) – Hybrid, Module PCB, RB

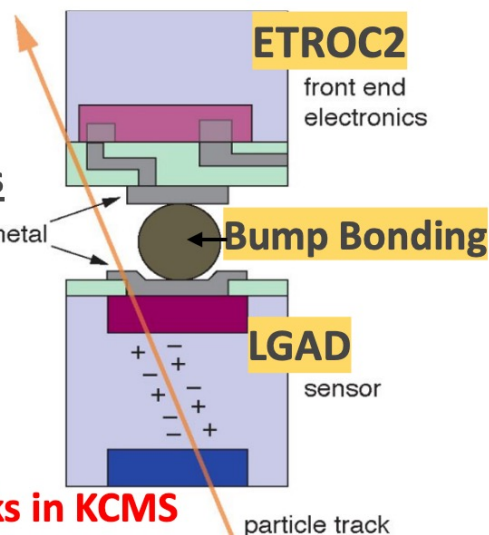
Hybrid (LGAD+ETROC)



Challenges:

Mechanical Robustness

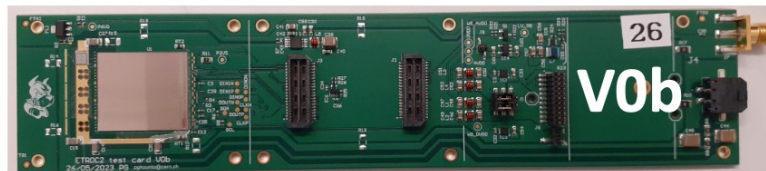
Thermal Reliability



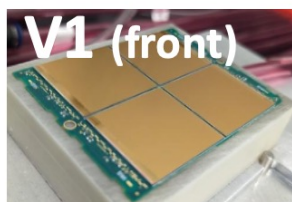
Ongoing works in KCMS

BB technique evaluation led by Dr. Jin Hyung Lee (KNU)

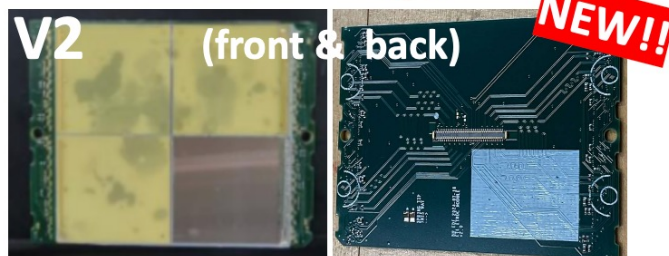
Module PCB



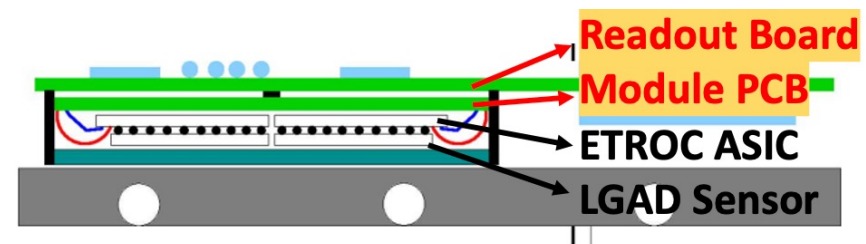
Early Prototype for initial test 16x16 ETROC, simple structure (~ 56 ps achieved)



1st Realistic Form-Factor (RFF) : Improved grounding & reduced noise ($\sim 55-80$ ps)



2nd RFF : Advanced design with separate power planes (Digital/Bias/Analog), noise reduction, enhanced Bias Voltage delivery
⇒ Target ≤ 50 ps time resolution

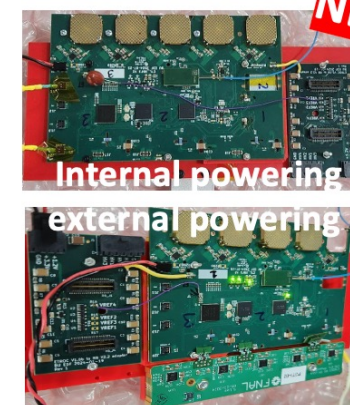


Readout Board (RB)

Connects ETROC to DAQ system (Optical fiber: VTRX+ protocol)



RB2 : Stable data transmission tested in system setup with Module V0b, V1 (stable, reliable)



RB Final 3 (RBF3) : Enhanced data throughput, firmware compatibility, and diagnostic features

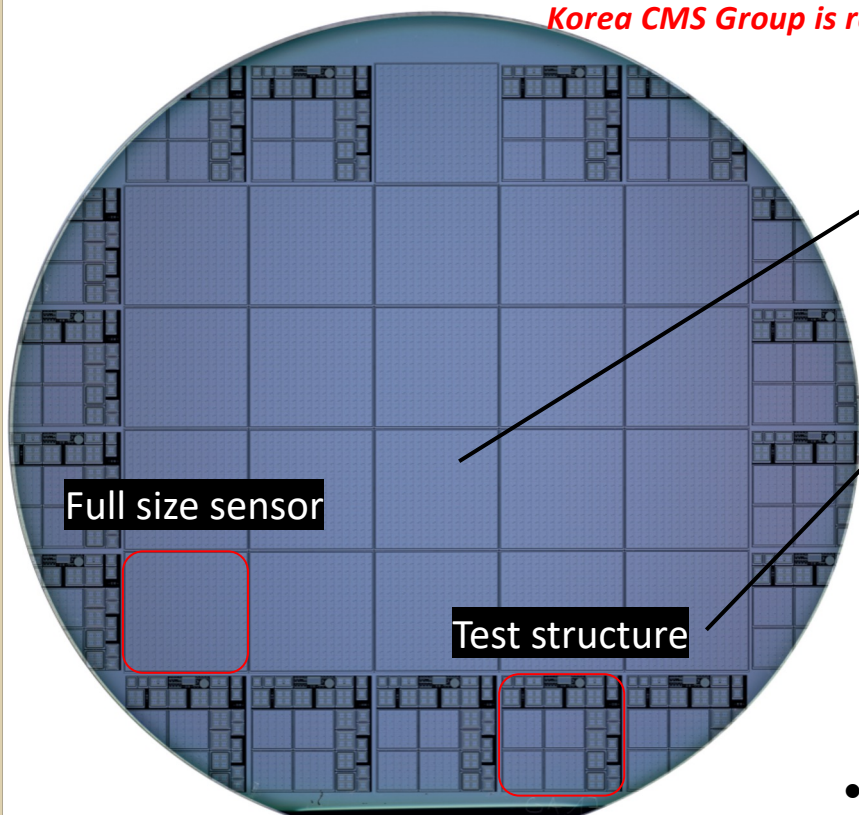
[RB upgrad](#)
[e Twiki](#)

Ultra-Fast Silicon Detector - Korea 1, 2 (UFSD-K1,K2)

• UFSD-K1 features the prototypes of the CMS Endcap Timing Layer

- KCMS and FBK (Italy) is cooperating for production of UFSD-K1, UFSD-K2 LGAD sensors
- UFSD-K1, UFSD-K2 wafers are post-processed in Korea.

Korea CMS Group is responsible for 25% of LGAD production for ETL.



UFSD-K1,K2 layout

• Full size sensor

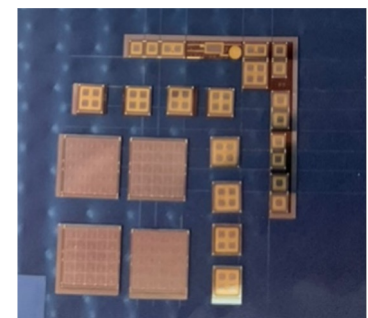
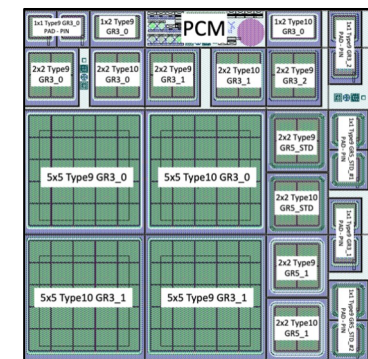
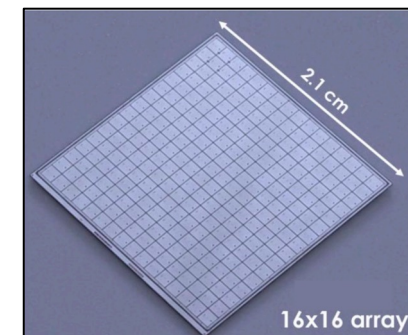
- 16x16 array LGAD (21 x 21 mm²)

• Test structure

- Under
- 1x1, 1x2, 2x2, 5x5 array LGAD sensors

• Wafer post-processing

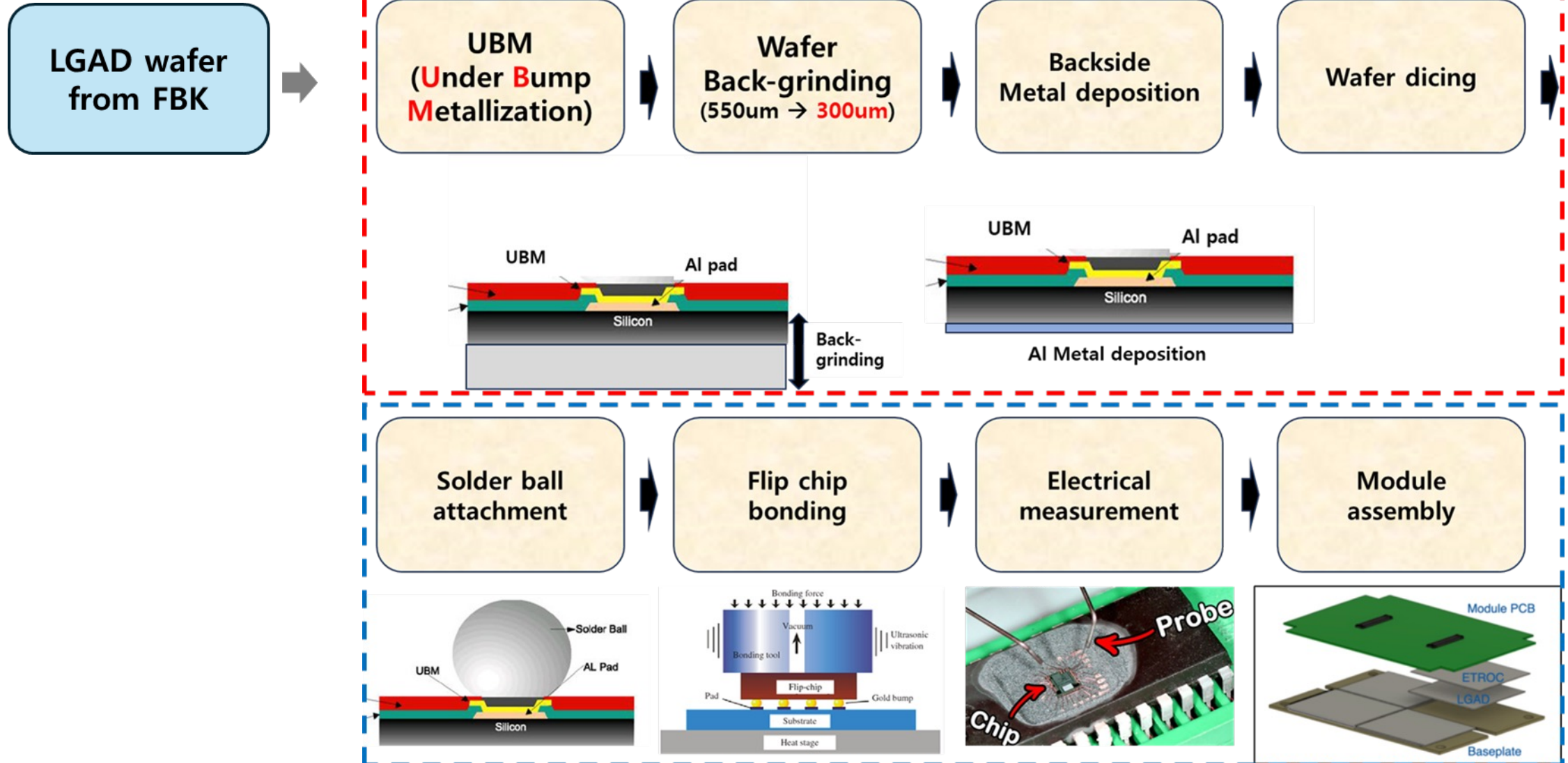
- Under Bump Metallization (Ni/Au)
- Backgrinding (300 μm)
- Back metal deposition (Al)
- Dicing



- Two 2x2 array K1 sensors were sent to Test Beam @ CERN SPS H6
- Some of the K1 sensors provided to other groups for further test.

LGAD wafer post-processing procedure in Korea

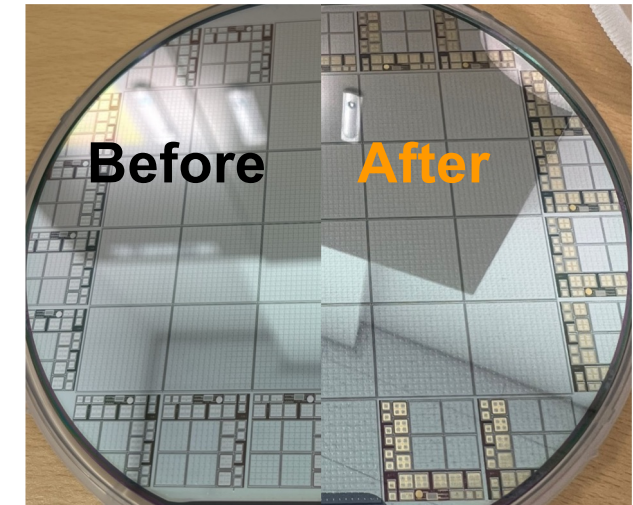
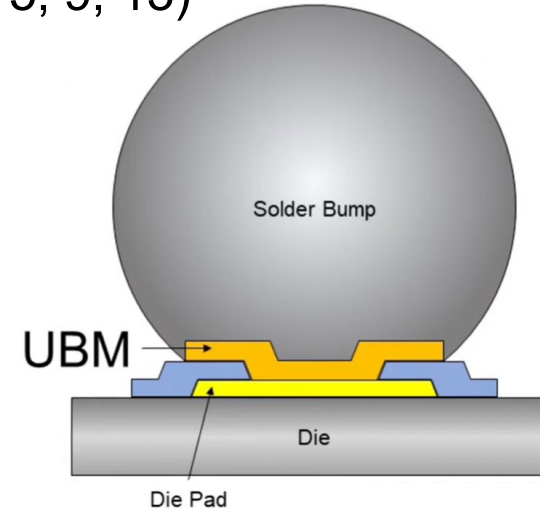
1) LGAD wafer post-processing



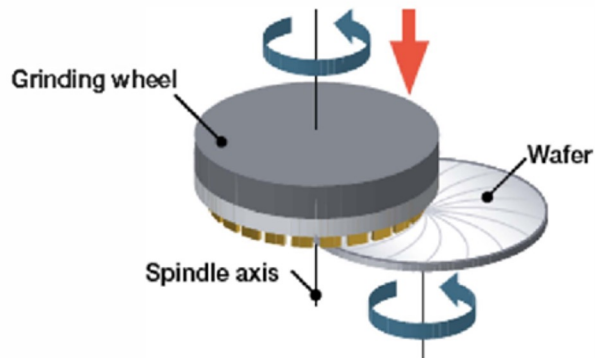
2) Bump bonding and module assembly

Wafer post-processing status in Korea

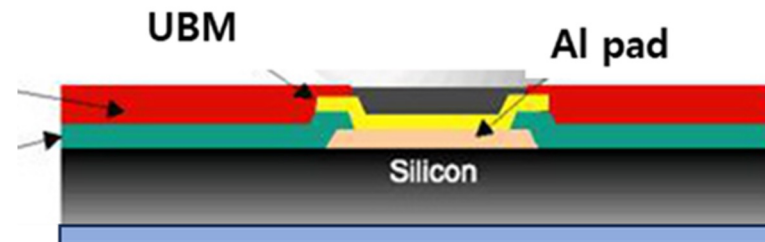
- Vendors from Korea completed post-processing and delivered to KNU.
 - Total 5 UFSD-K1 wafers
 - UFSD-K1 standard supplier wafers(# 1, 5, 9, 13)
 - One new supplier wafer (# 6)
 - One UFSD4 No. 14 wafer
- UBM process proceeds with electroless plating
 - Thin film metal layer (Ni/Au) stack
- Backgrinding thickness = 300 μm
- Al used for backside metalization
- Dicing done with 16x16 sensor size (21mm x 21mm)



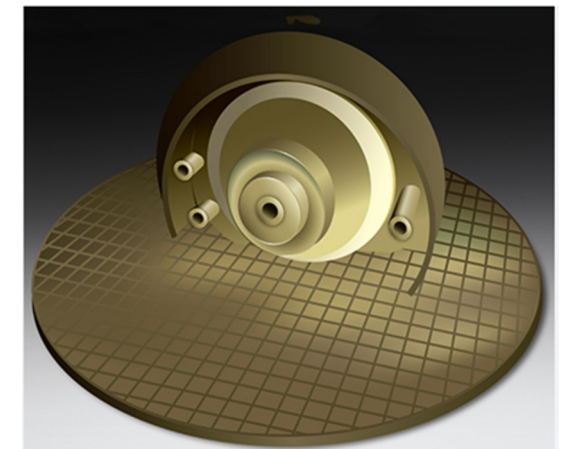
1) UBM before & after



2) Backgrinding



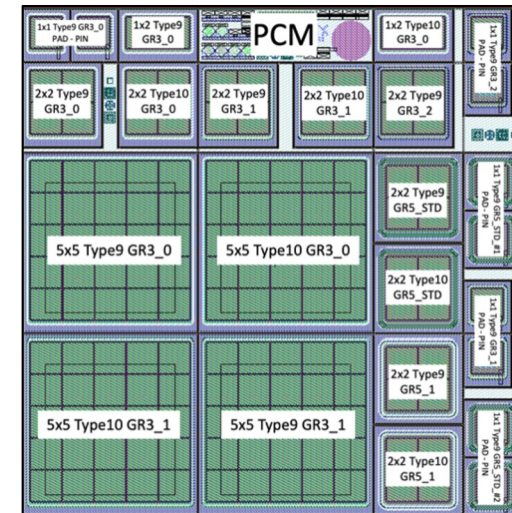
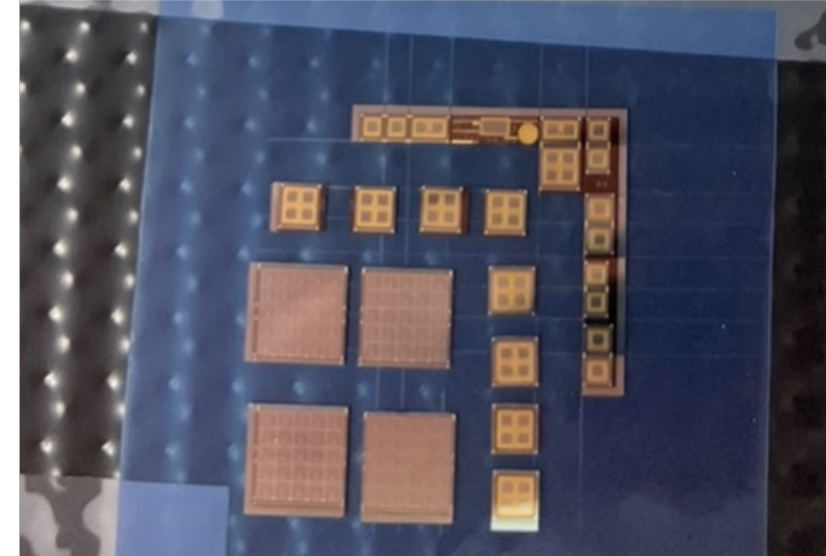
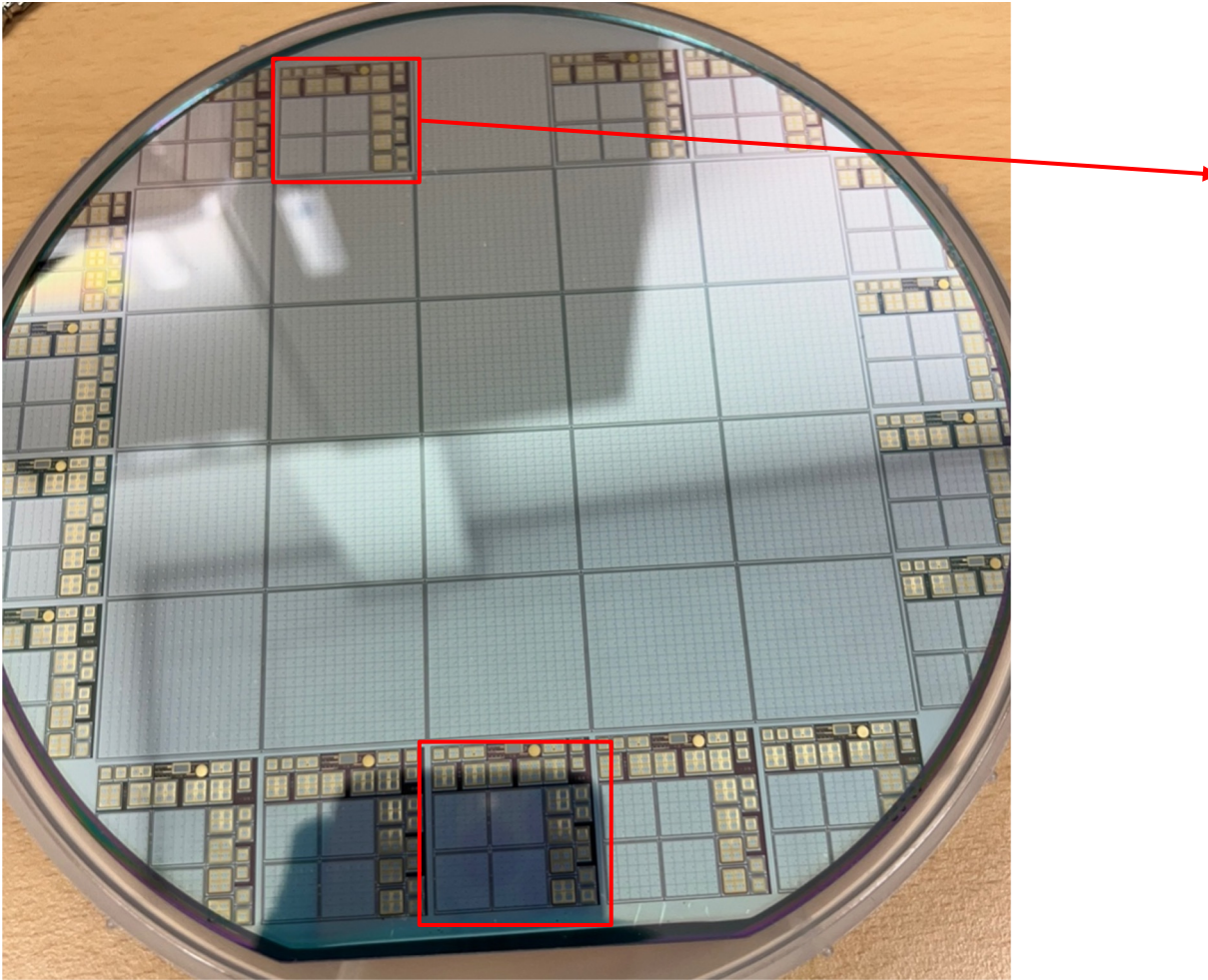
3) Al backside metalization



4) Dicing

Wafer post-processing status in Korea

- Two test structures in each wafer were diced in detail.

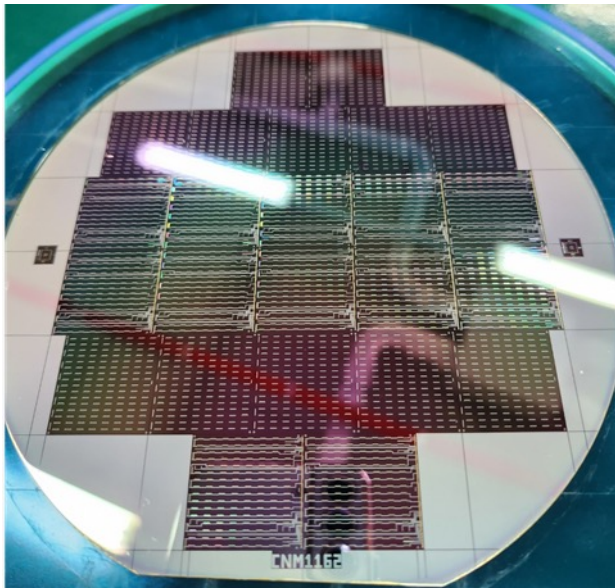


Fabrication of dummy wafer for bump-bonding test

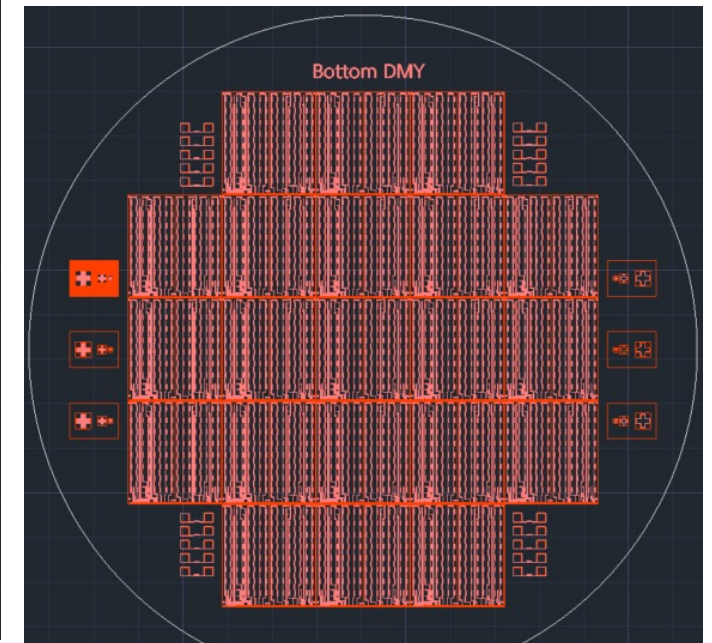
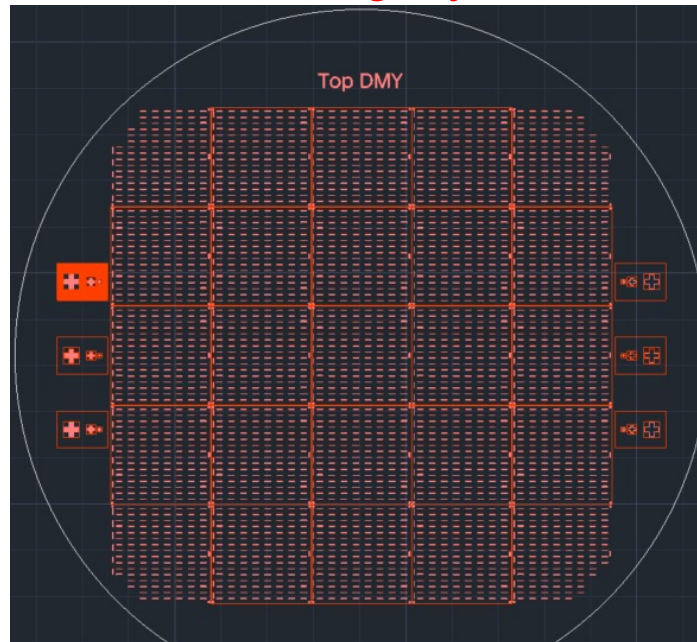
I designed the dummy wafers by myself and fabricated them at the ETRI fab in Korea.

- ❑ To verify the yield of the bump bonding process on a large scale.
- ❑ The dummy wafers have different sizes for the top and bottom parts compared to the Kansas University wafers.
 - To facilitate the dicing process.
 - Therefore, we made separate photomasks for the top and bottom parts.
- ❑ Each wafer consists of **21 main chips** and test patterns on the wafer.

6 inch wafer image of the Univ. of Kansas



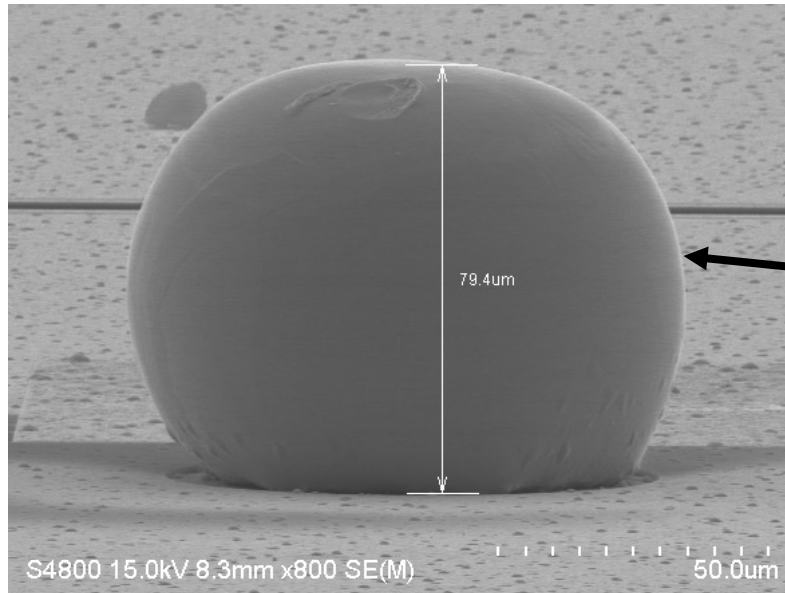
6 inch wafer design by KCMS team for dummy wafer fabrication in Korea



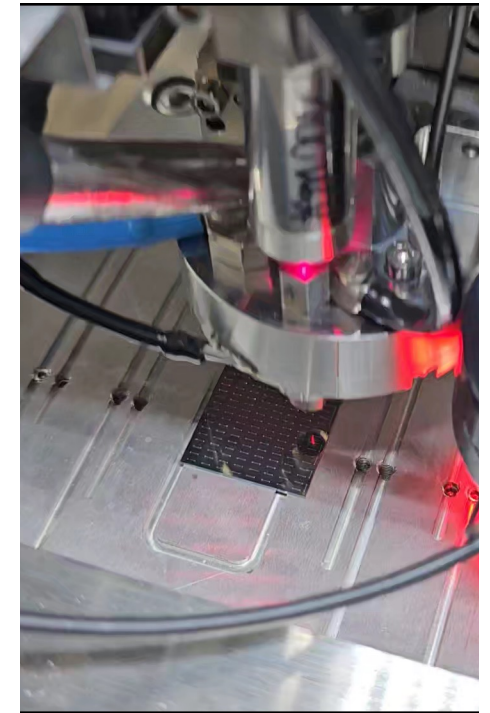
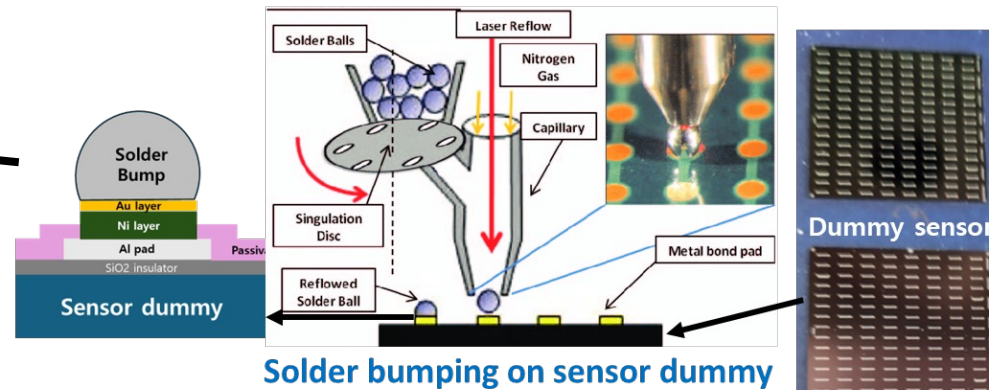
Solder ball attachment test on dummy sensors

- Attempting three types of solder bumping process
 - **Laser reflowed solder ball**

[SEM image]



Method1 : Solder bumping by laser reflowed solder ball]

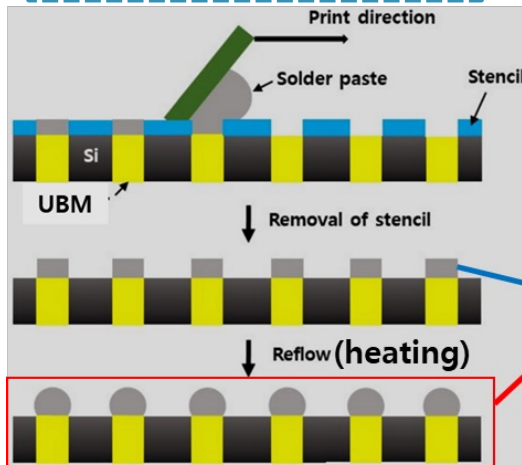


- Solder bump height of $\sim 80\mu\text{m}$ (using $100\mu\text{m}$ diameter ball)
- Good uniformity of the formed solder bump
 - Out of a total of 272 pads, solder loss is minimal and, if present, is at most 1 or 2 pads

Solder ball attachment & bump-bonding process

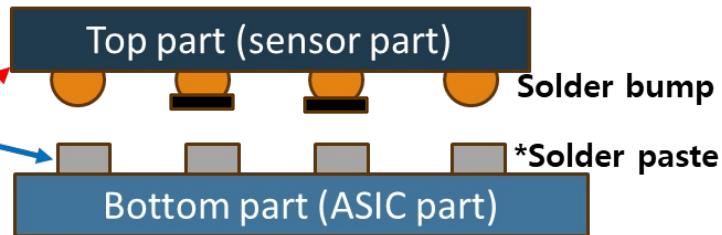
Method 2: Solder paste printing & Bump-bonding process (at [Hansol Semiconductor](#))

1) Solder bump formation on sensor chip

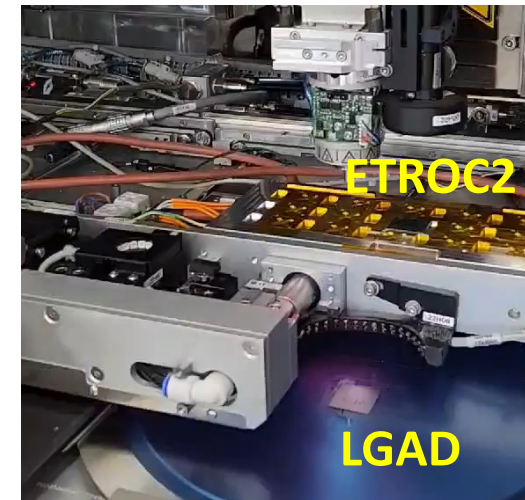


2) Solder paste printing on ETROC2 chip

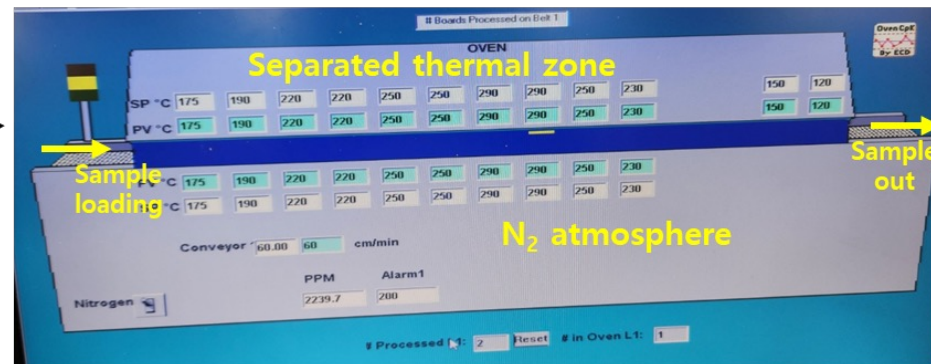
*Solder paste, with its **slight stickiness**, temporarily holds the solder bumps in place until soldering is completed.



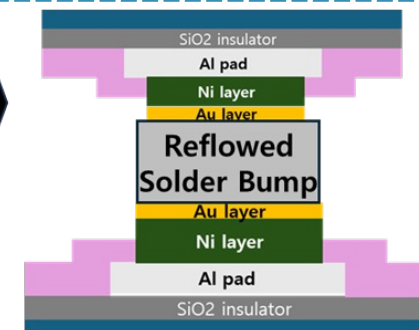
3) Bump-bonding using flip-chip bonder (~10 sec/sample)



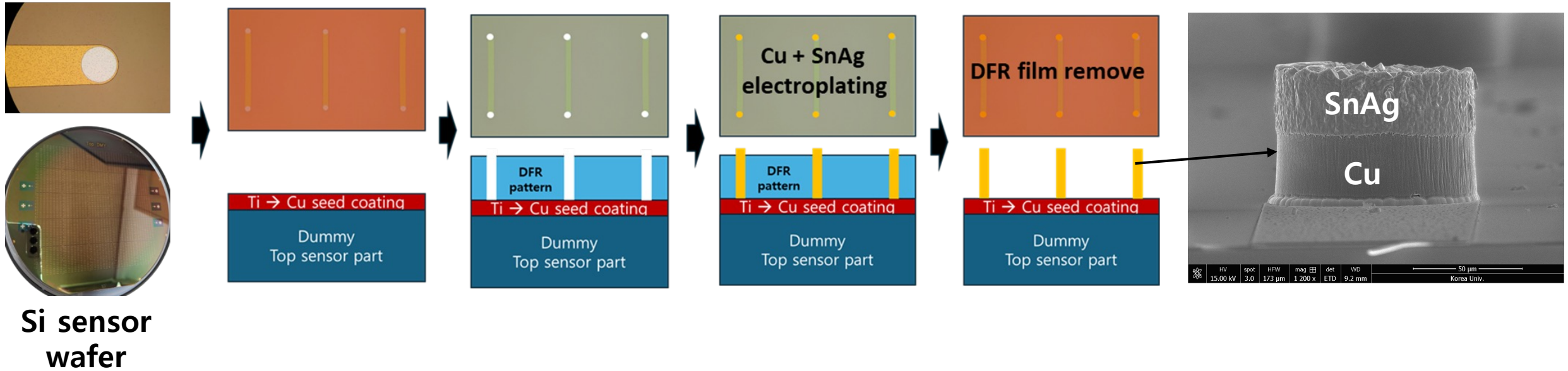
4) Solder reflow process for bump solidification



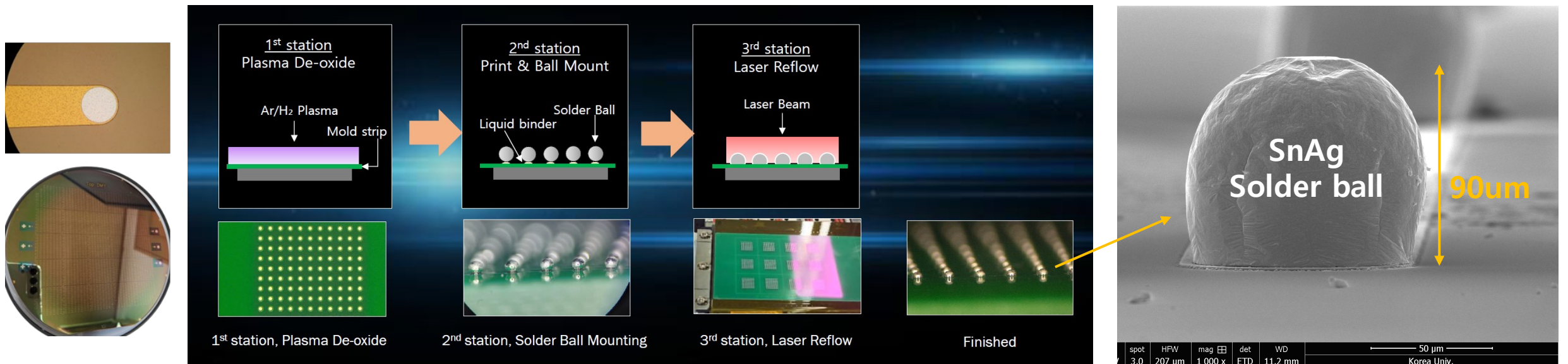
5) End of bump bonding process



Method 3: [Electroplating process for solder bump formation]

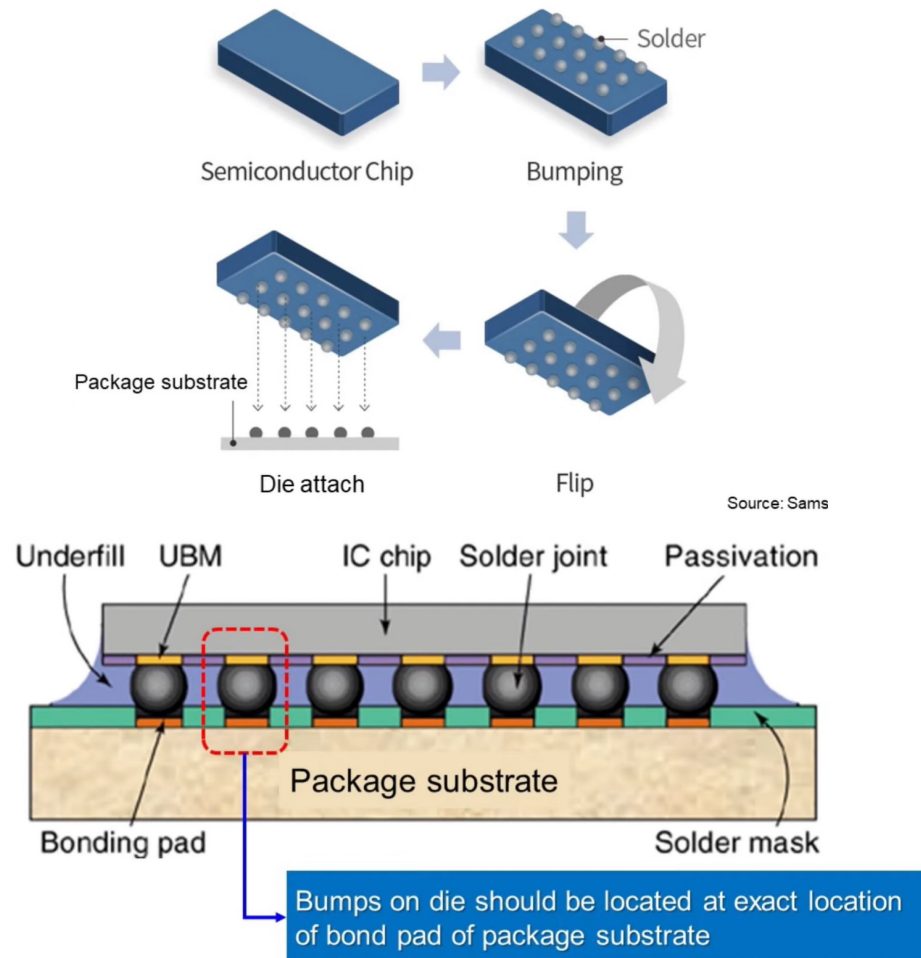


[Solder ball attachment process for mass production of solder bump]

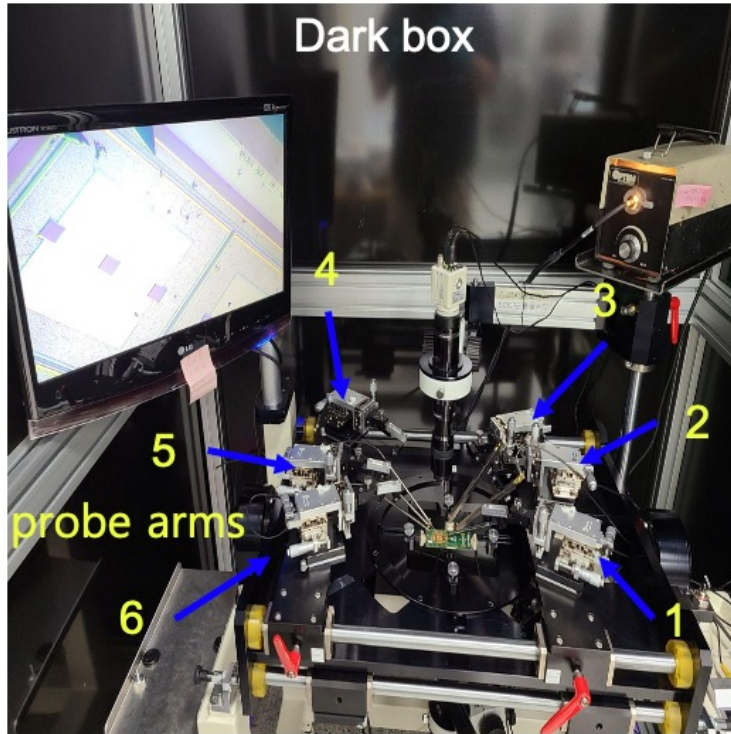


Bump-bonding / Flip-chip bonding process

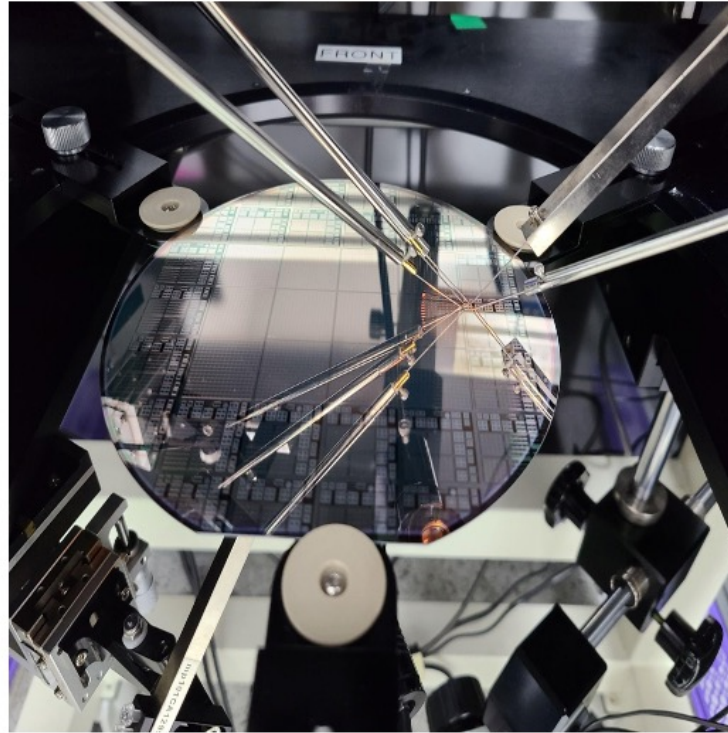
- Bump/Flip-Chip Bonding is a process that creates a bump on the chip to make an electrical/mechanical connection with the chip/substrate.



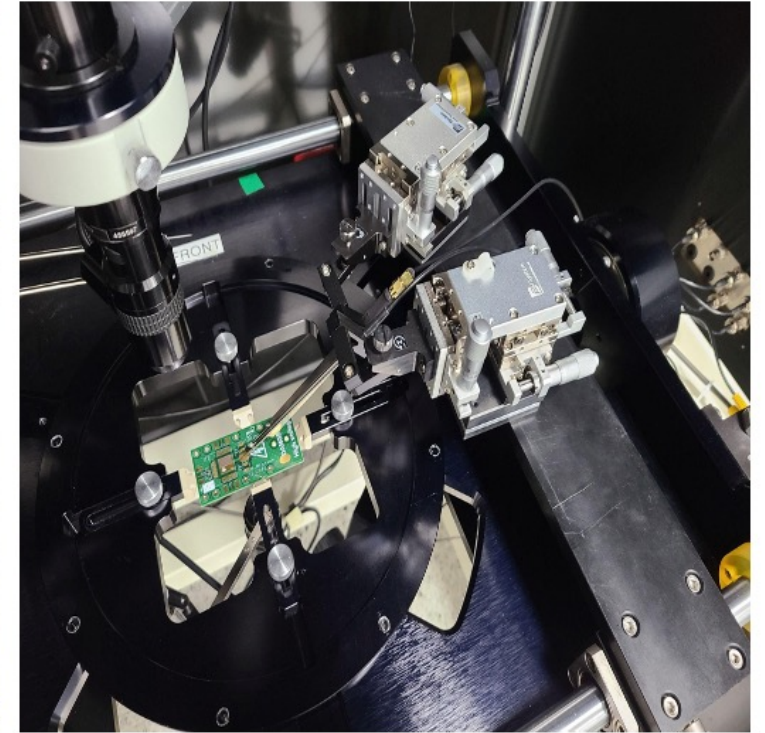
Probe station setup for wafer-level and sensor-level tests



● Overview



● wafer tray

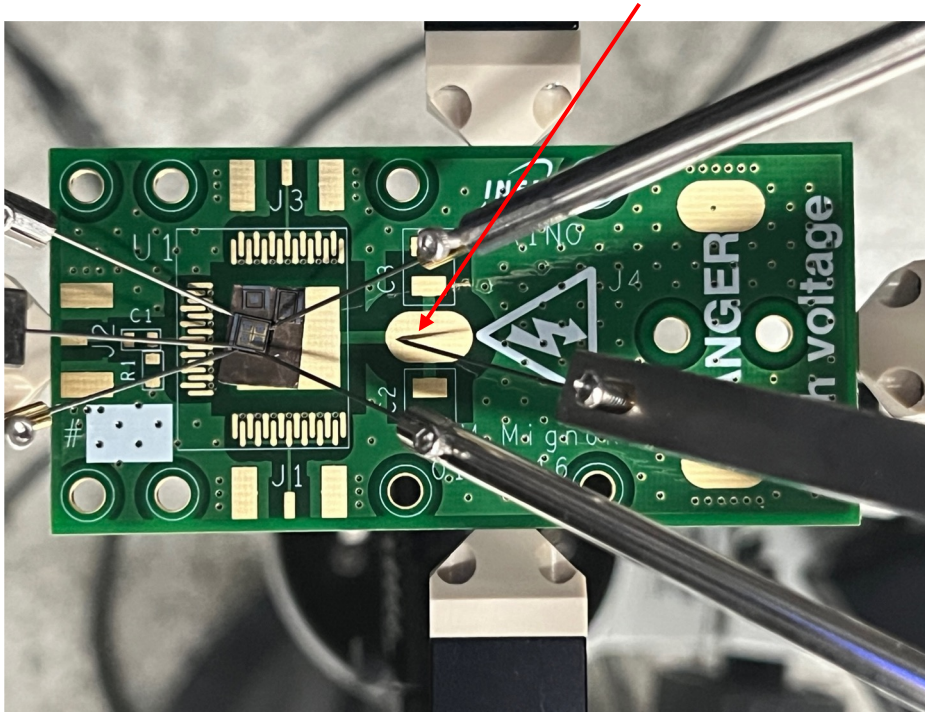


● sensor tray

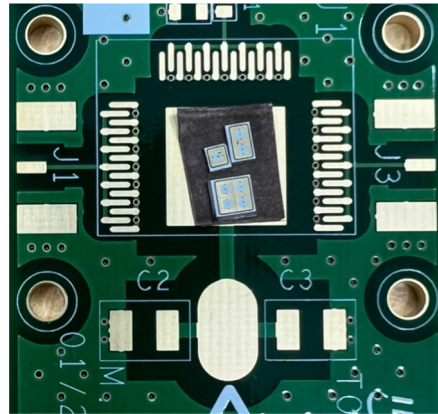
- There are **6 probe arms** that use magnets to connect with the station (1 for signal read-out, 1 for bias voltage supplying, and 4 for grounding)
- Two types of tray available for wafer-level and sensor-level tests
- KCMS currently has plan to prepare a **probe card** and **switching matrix for 16x16 sensors**

Sensor level test at KNU

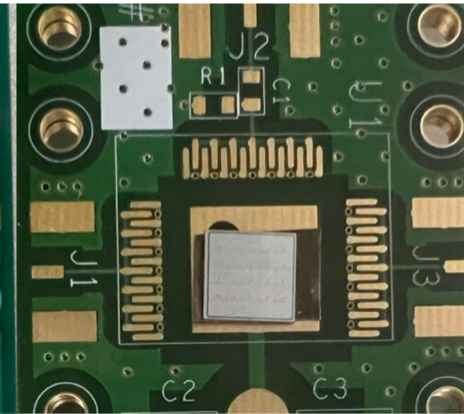
Bias voltage apply



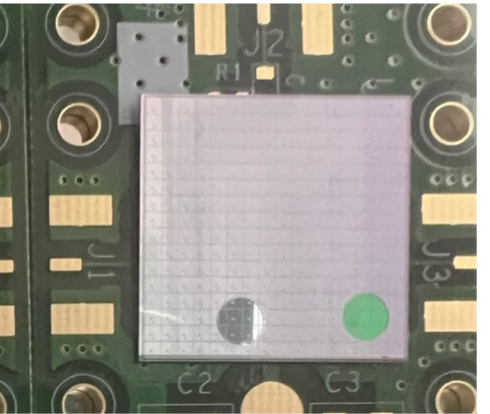
1x1, 1x2, 2x2



5x5

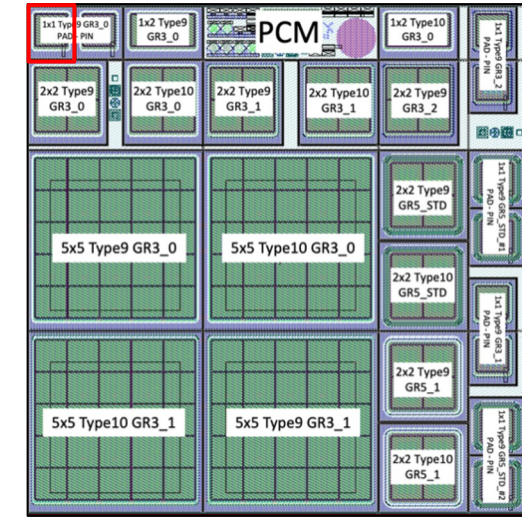
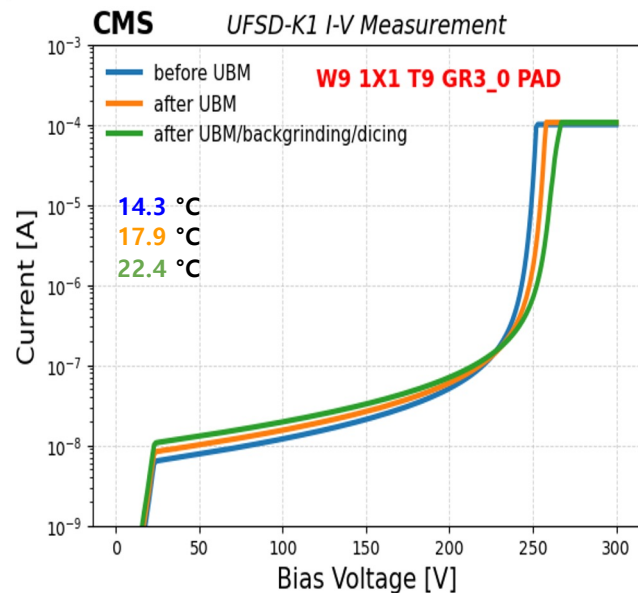
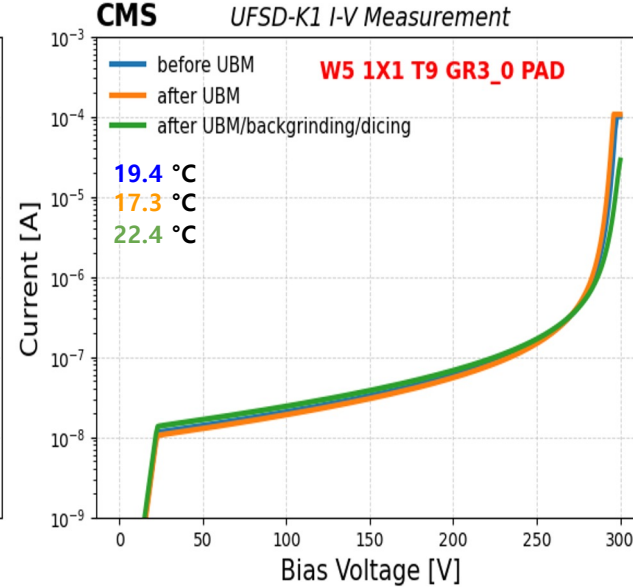
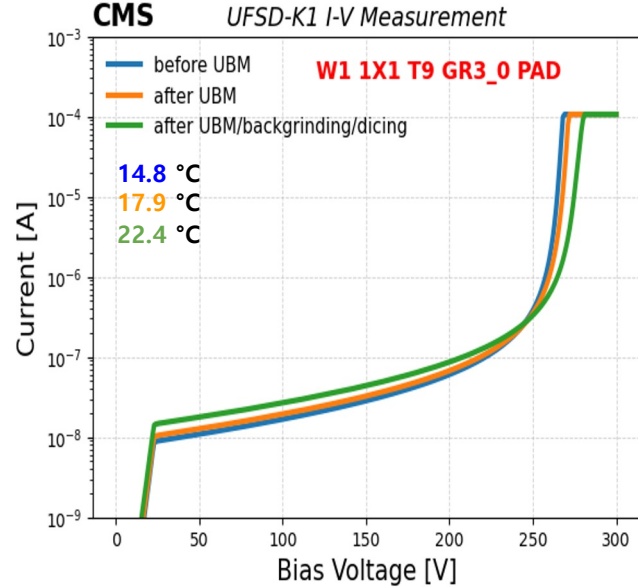


16x16



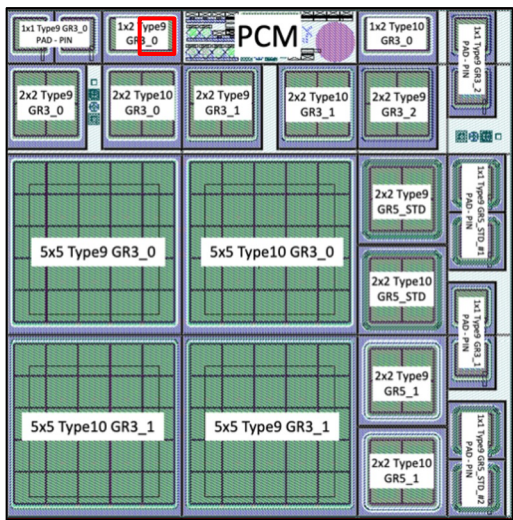
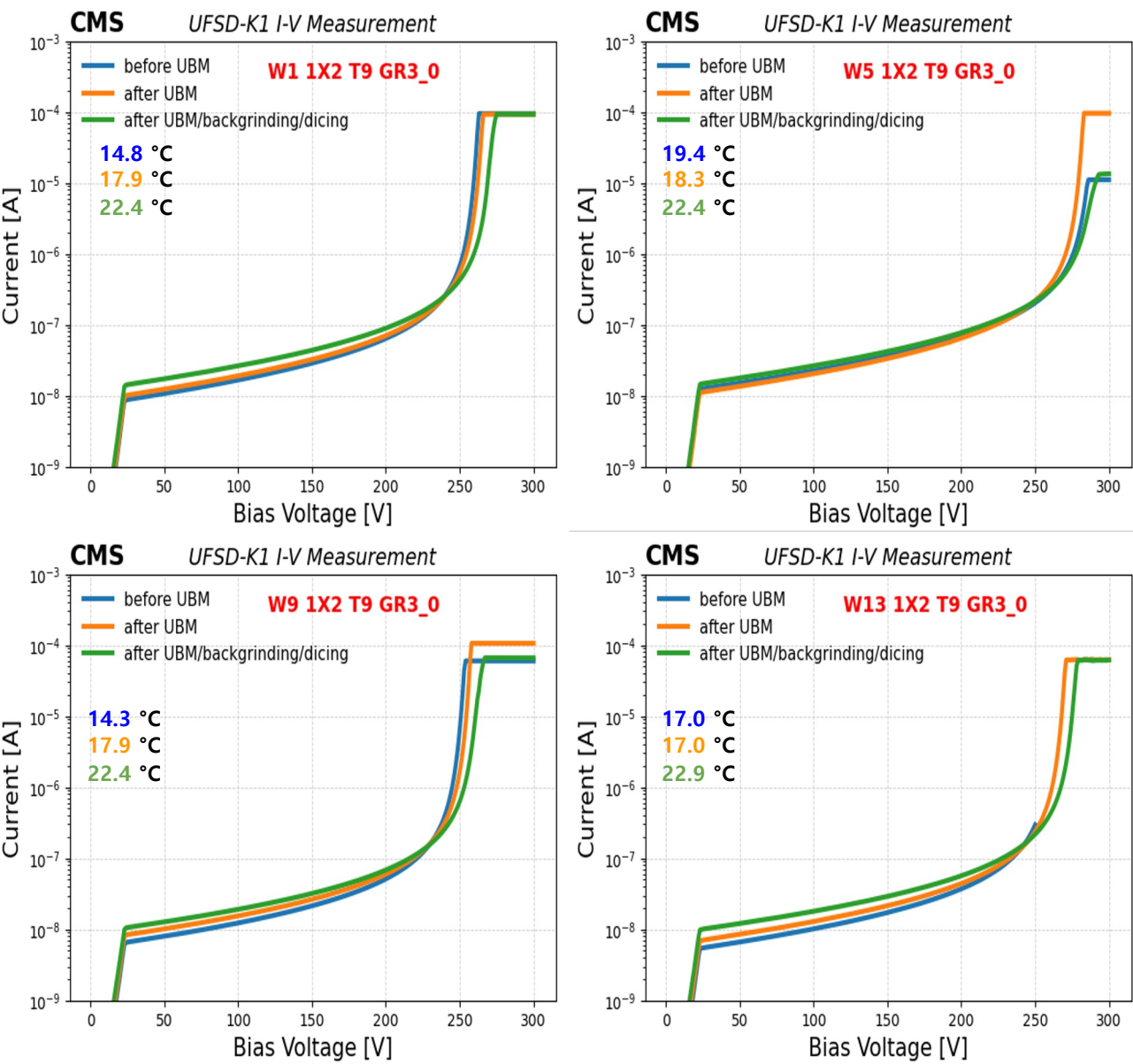
- Sensors can be attached to PCB board with electrically conductive double sided tape.

I-V results comparison before and after UBM : 1x1 size (PAD)



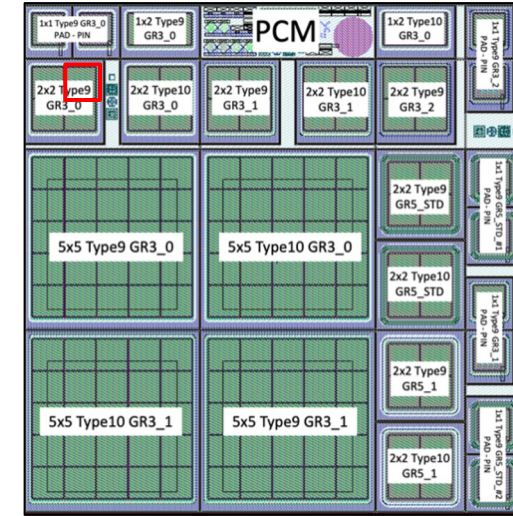
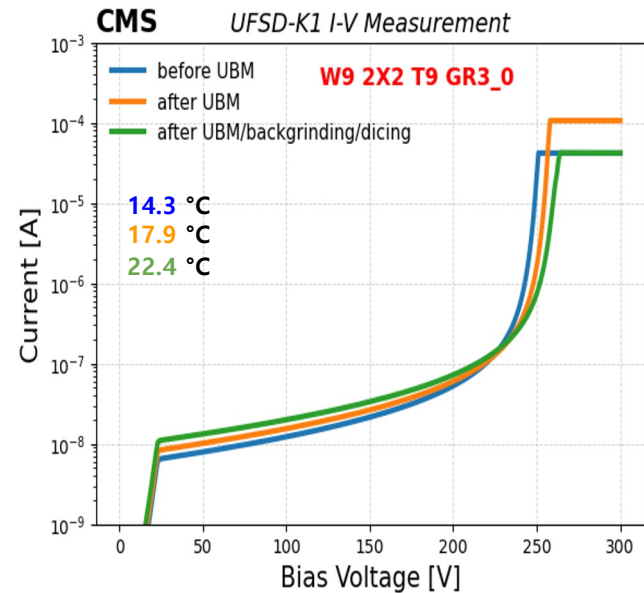
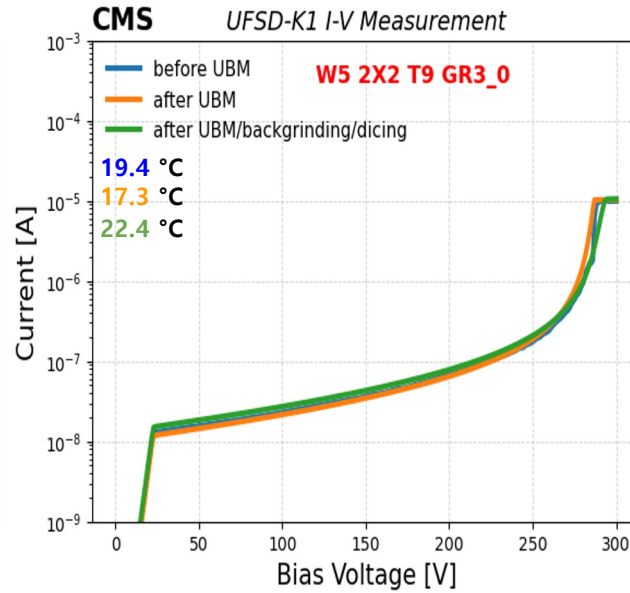
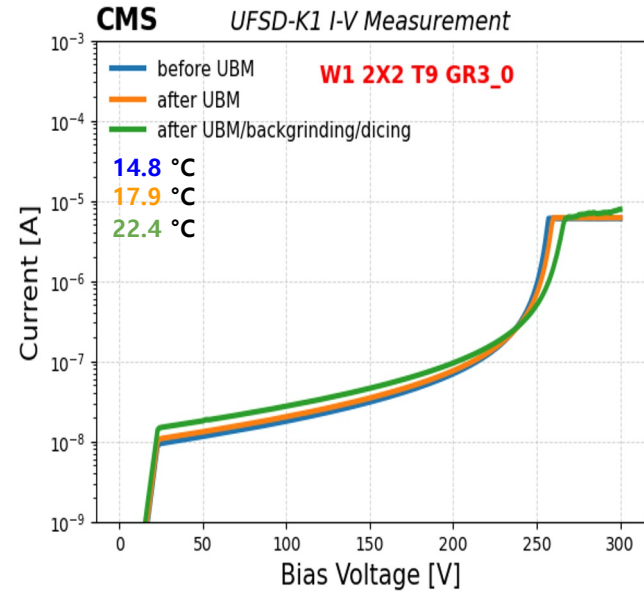
- Current limit = 100 μ A
- Bias Voltage applied up to 300 V
- Current increased after post-processing

I-V results comparison before and after UBM : 1x2 size



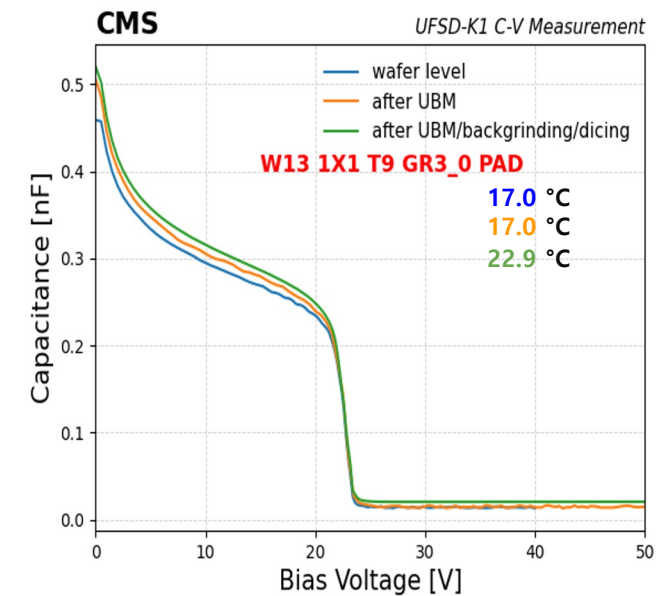
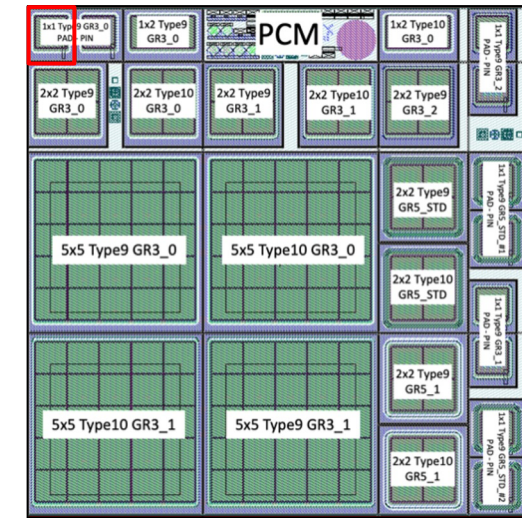
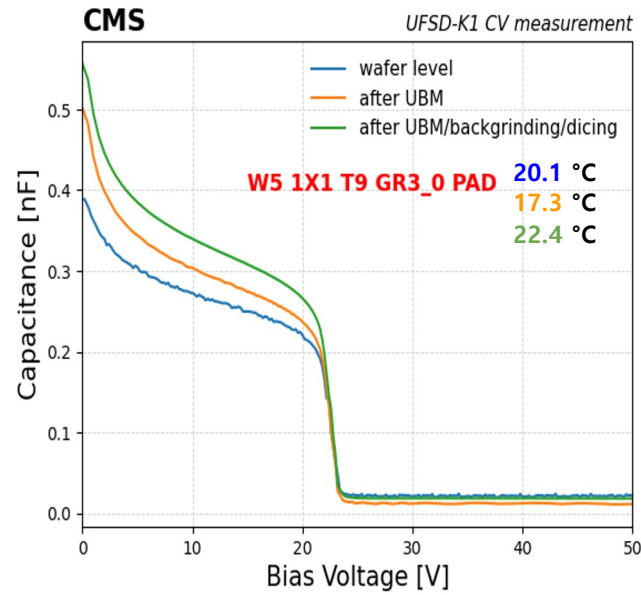
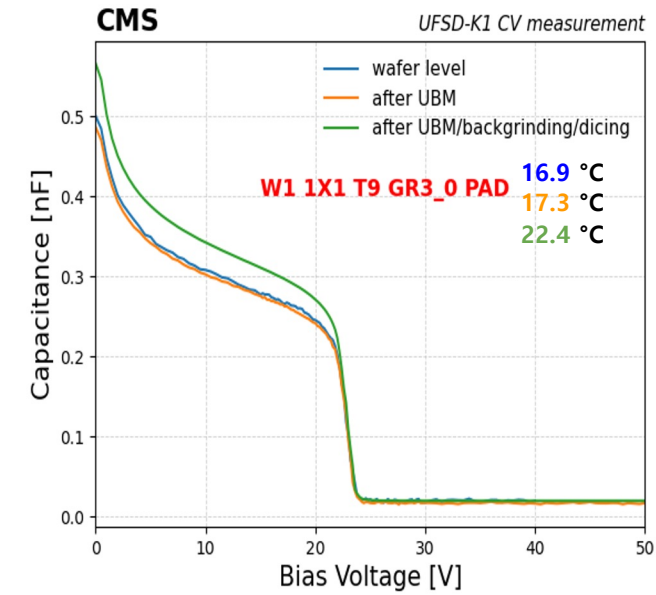
- Grounded other pad during measurement
- Current increased after post-processing

I-V results comparison before and after UBM : 2x2 size



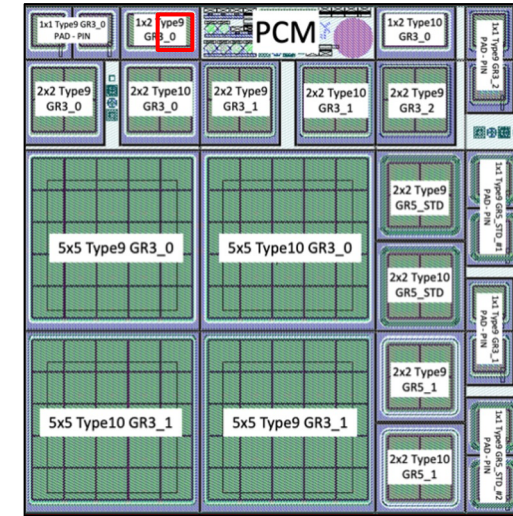
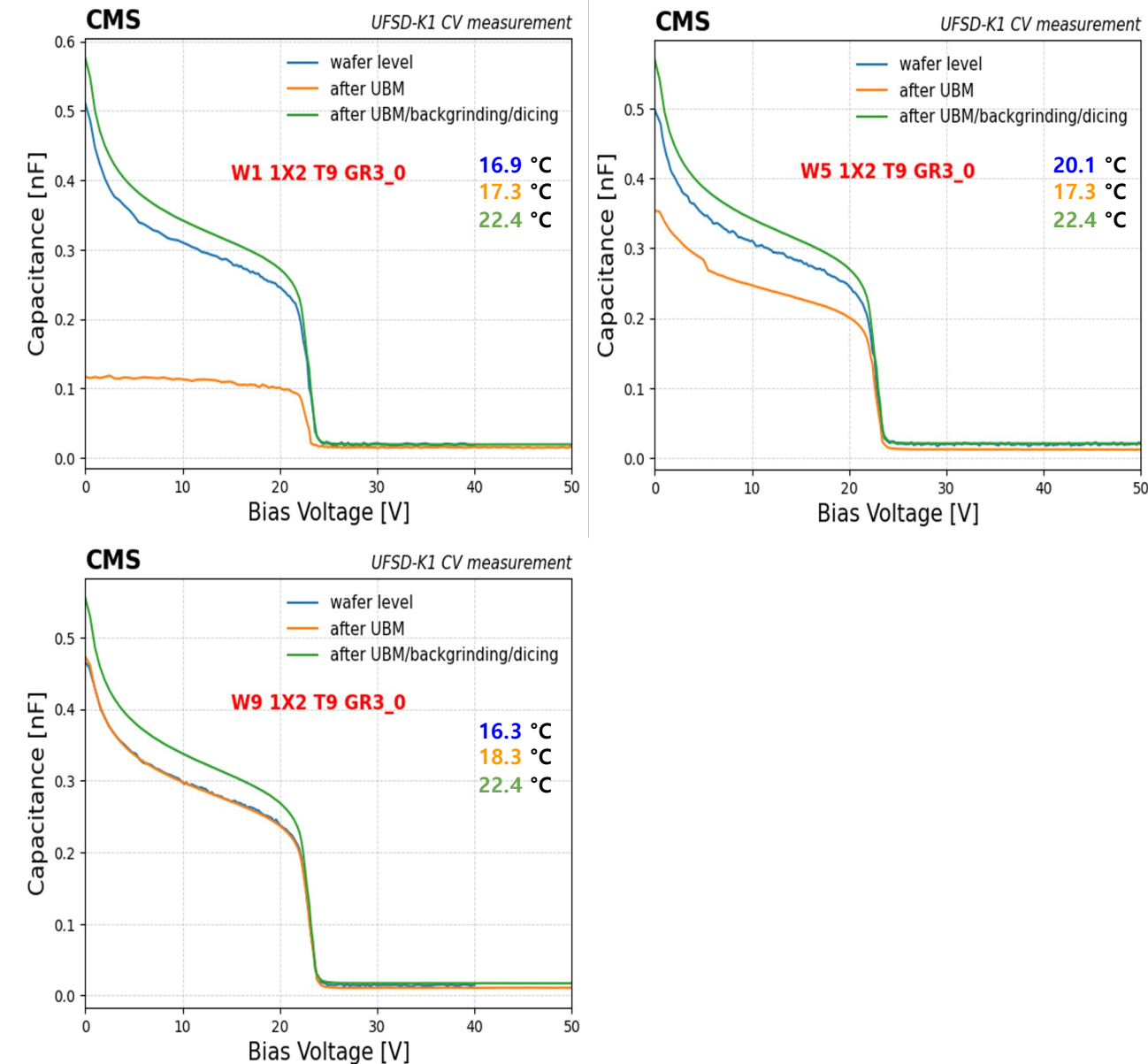
- Grounded other pads during measurement.
- Current increased after post-processing

C-V results comparison before and after UBM : 1x1 size (PAD)



- Bias voltage applied up to 60 V
 - $V_{fd} \sim 24V$
- V_{fd} is consistent before and after the UBM.
- Difference capacitance below V_{fd}

C-V results comparison before and after UBM : 1x2 size

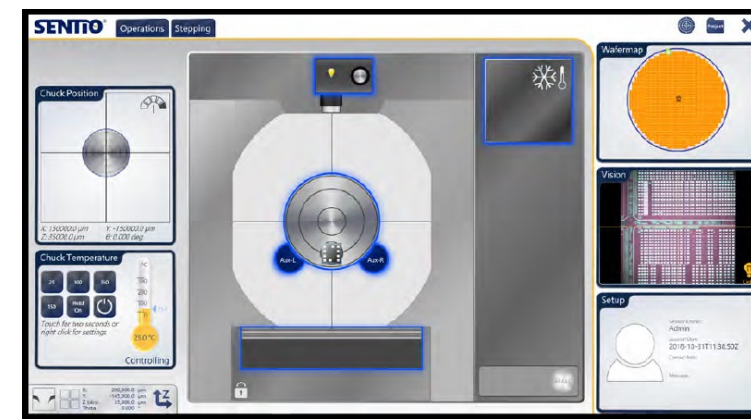


- Bias voltage applied up to 60 V
 - $V_{fd} \sim 24V$
- V_{fd} is consistent before and after the UBM.

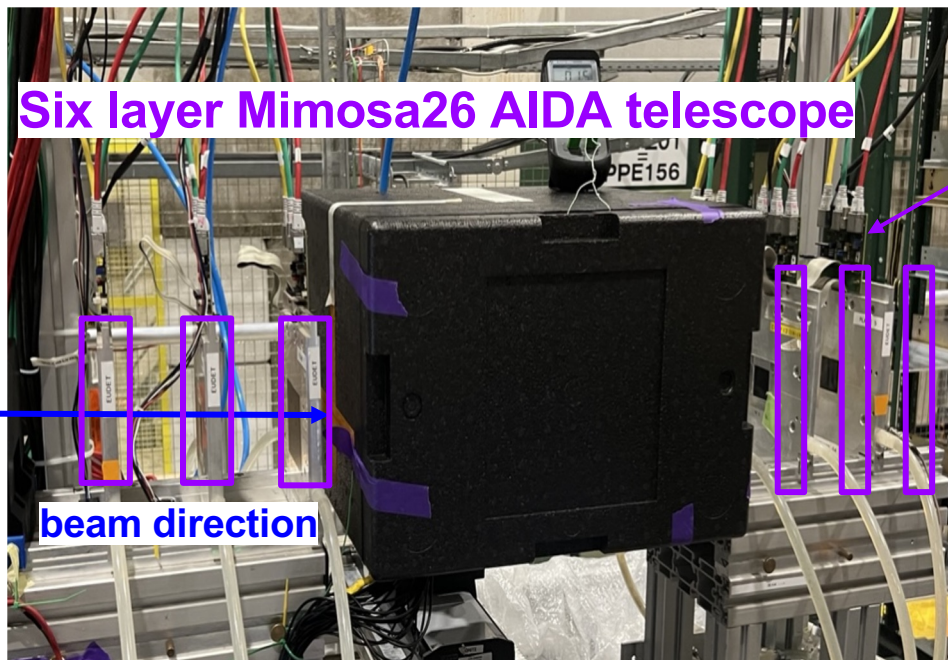
Key features

- **IceFreeEnvironment™**

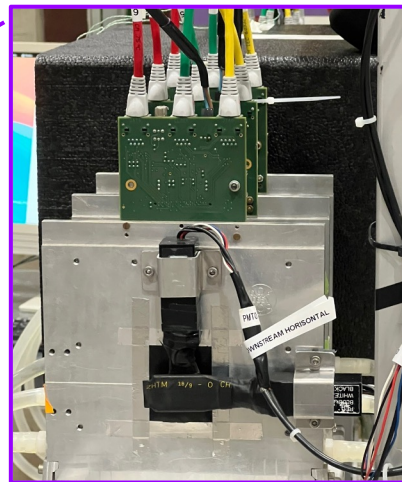
- Enables ice-free measurements down to -40°C using both probe cards and micro-positioners simultaneously.
- Guarantees stable low-temperature operation without condensation.
- **ERS AirCool® PRIME Thermal Chuck**
 - Temperature range : $-40^{\circ}\text{C} \sim +150^{\circ}\text{C}$
- **Integrated Hardware Control Panel & Touchscreen**
 - Intuitive operation for chuck control and system status monitoring.
- **Active Vibration Isolation Table**
 - Ensures stable micro-positioning and accurate probe contact.
- **MPI SENTIO® Software Suite**
 - Multi-touch, smartphone-like operation for prober and microscope control.
- **DarkBox Option**
 - Light-tight enclosure for photo-sensitive device testing. Probe card mounting



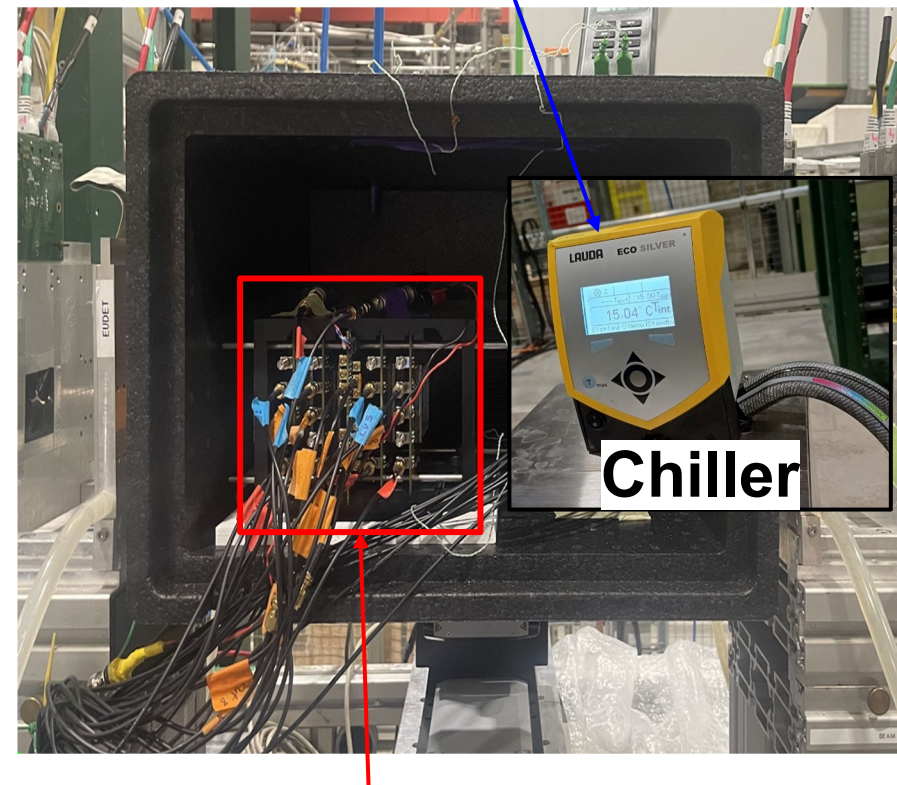
Test Beam @ CERN SPS H6



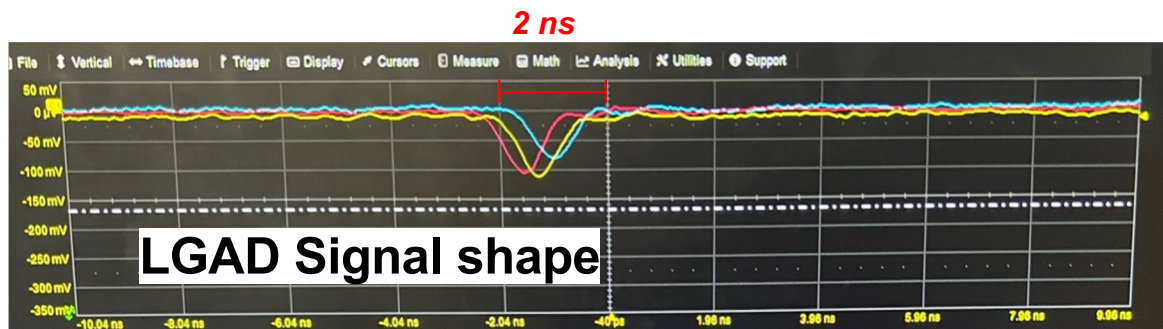
Right side



Chiller used for constant temperature at 15 °C



Mimosa26 telescope were used for beam quality check & tracking
(left : 3 layer telescope, middle : dark box, right : 3 layer telescope)



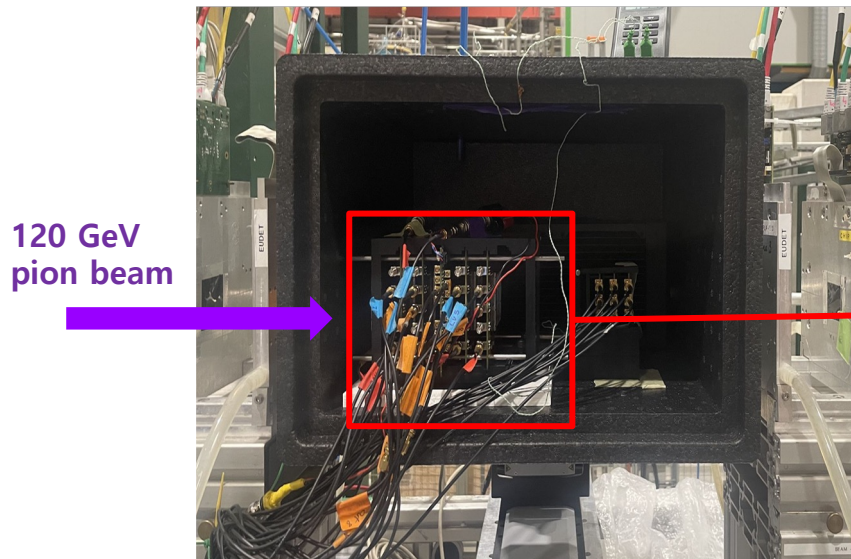
Datas are acquired with 8 channel oscilloscope

6 Santa-Cruz boards are located in the test module

- Two UFSD-K1 2x2 array LGAD sensors
- Four UFSD-LF 1x1 LGAD sensors

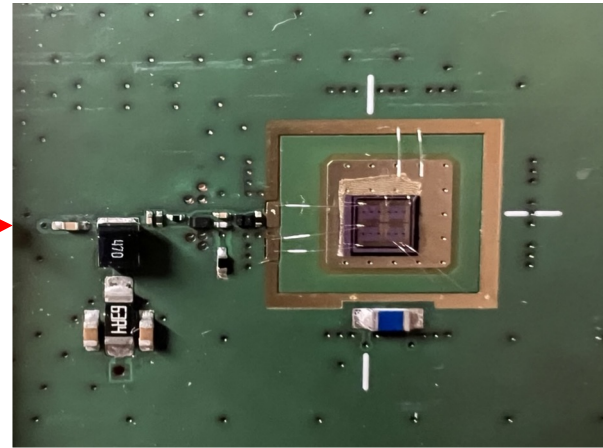
Test Beam Results for LGAD sensors at CERN

- Test beam were carried out by KNU and Torino group at SPS H6



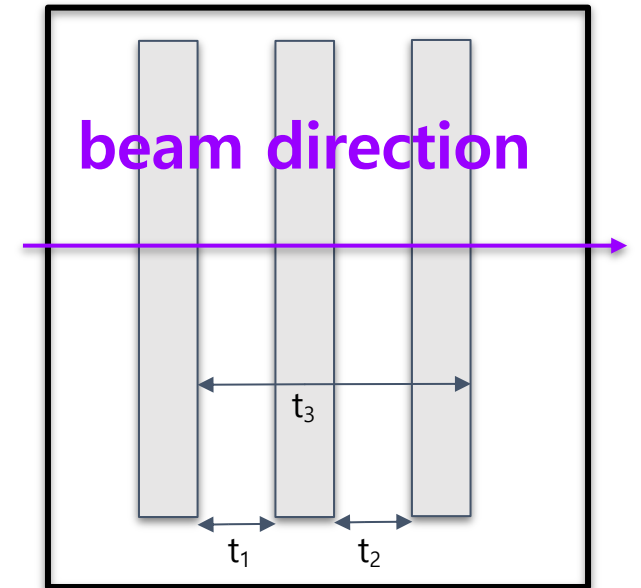
Dark box chilled to 15 °C

UFSD-K1 2x2 (T9 GR3_0)



PCB wire bonding layout

Telescope in Dark box



- Time resolution of each sensors are extracted by following formula

$$\sigma_i^2 = (\sigma_{i,j}^2 + \sigma_{i,k}^2 - \sigma_{j,k}^2)/2$$

$$i \neq j \neq k$$

$$i, j, k \in [1,2,3]$$

$$\sigma_1 = \mathbf{32.34 \text{ ps}}$$

$$\sigma_2 = \mathbf{35.04 \text{ ps}}$$

$$\sigma_3 = \mathbf{33.30 \text{ ps}}$$

LGADs has been reached
35 ps timing resolution.

Irradiated LGAD sensors at KOMAC in Korea

KOMAC (Korea Multi-purpose Accelerator Complex)

TR23 (20 MeV versatile beamline)

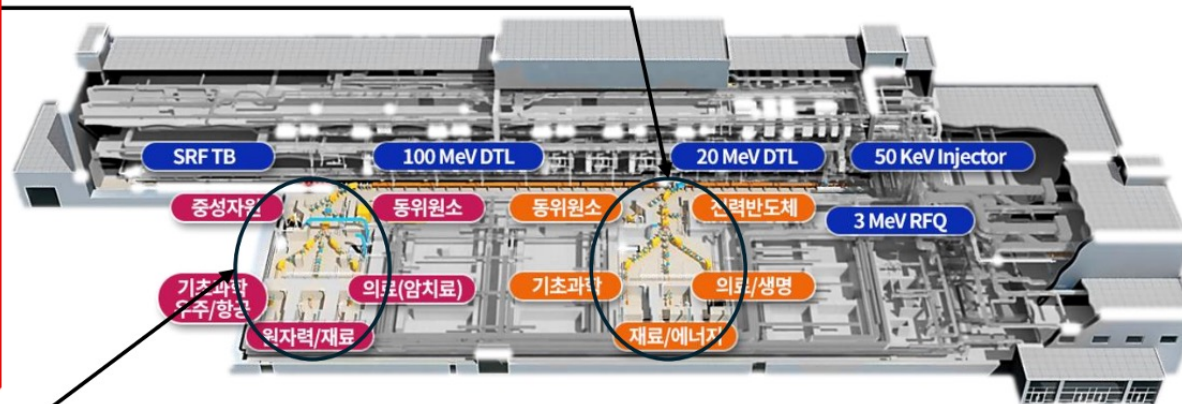
A research facility where materials or products are irradiated with a proton beam accelerated up to 20 MeV under various conditions.

High-dose proton beam research facility



Specifications of the TR23

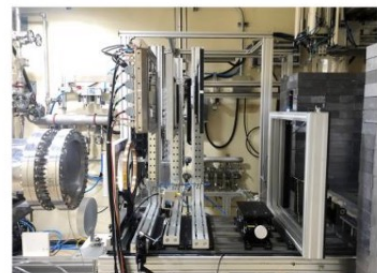
Energy	15 - 20 MeV
Beam Current	1 ~ 10 mA
Beam Flux	$1E10 \sim 1E11$ #/cm ² /pulse
Irradiation Area	30 mm- ϕ
Quality standards (ISO 9001)	Fluence: $\pm 10\%$ Uniformity: $\pm 10\%$ Energy: $\pm 5\%$
Application fields	Materials, Nuclear Physics, Semiconductors, etc.



TR103 (100 MeV versatile target room)

A research facility for irradiating materials or products with a proton beam accelerated to 100 MeV under various conditions.

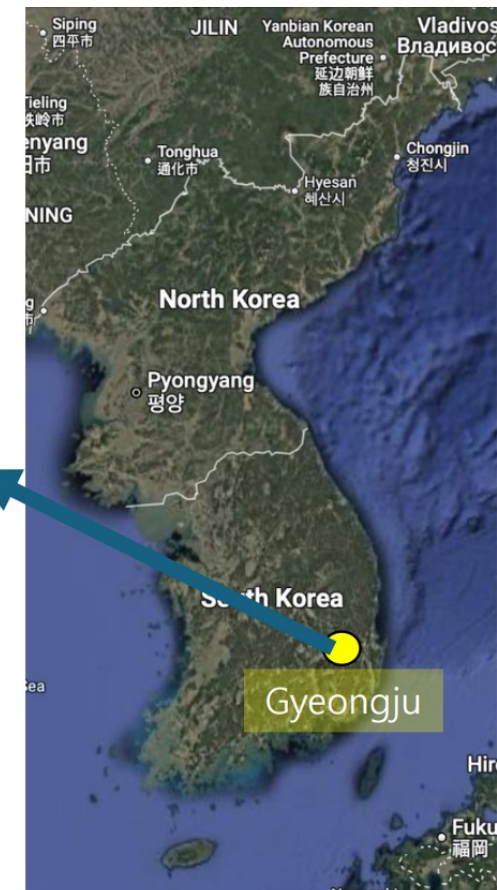
High-dose proton beam research facility



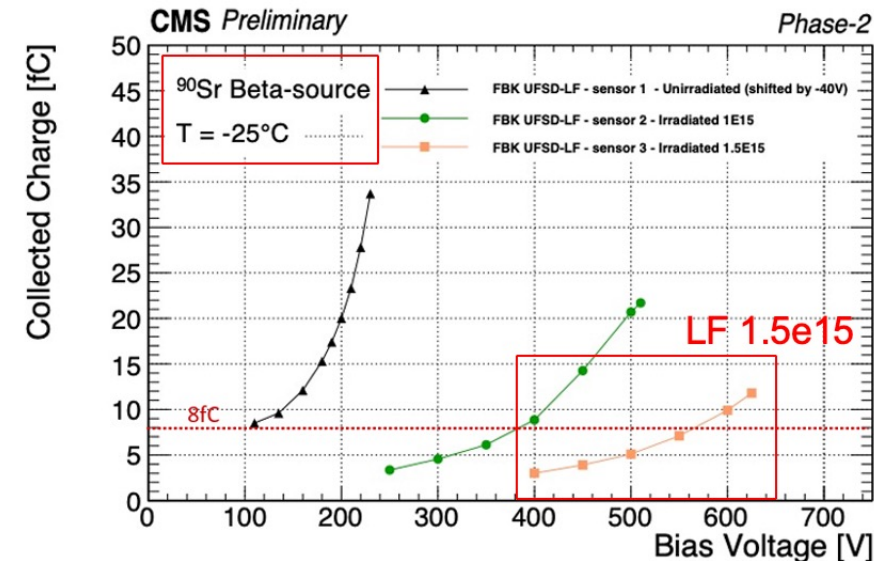
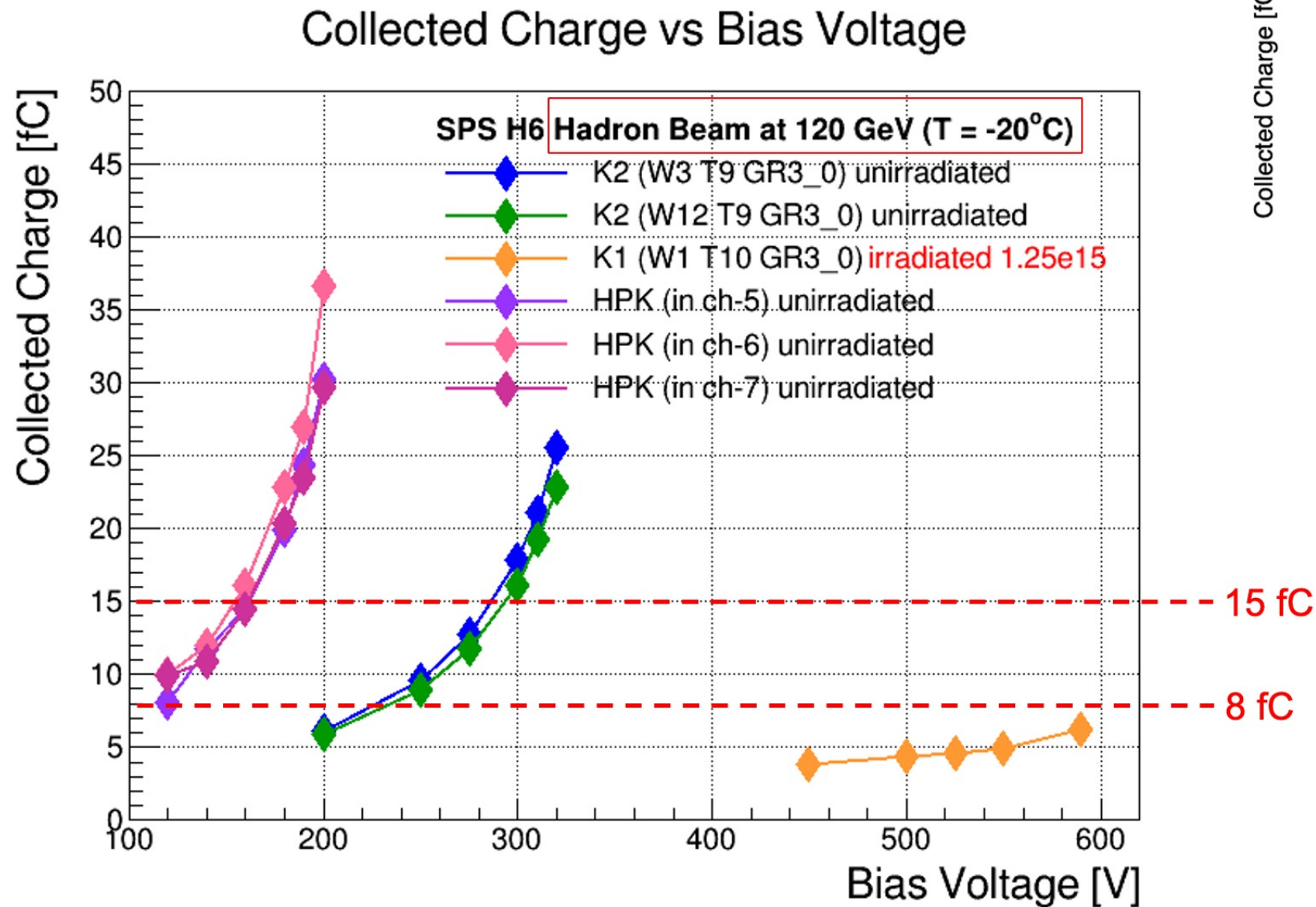
Specifications of the TR103

Energy	30-100 MeV
Beam Current	1-10 mA
Beam Flux	$1E10 \sim 1E11$ #/cm ² /pulse
Irradiation Area	30 mm- ϕ
Quality standards (ISO 9001)	Fluence: $\pm 10\%$ Uniformity: $\pm 10\%$ Energy: $\pm 5\%$
Application fields	Biotechnology, materials, nuclear physics, semiconductor

- For both room, beam flux would be $1E10-1E11$ /pulse
 - Depend on the beam status
 - Beam size: 30 mm ϕ
 - insure the fluence within 10% uncertainty
 - Outside the area beam is still active
 - only use single sample per each irradiation
- With 100 MeV beam, deposited dose is so small and expect larger irradiation time
 - Decide to use 20 MeV beamline (TR23)



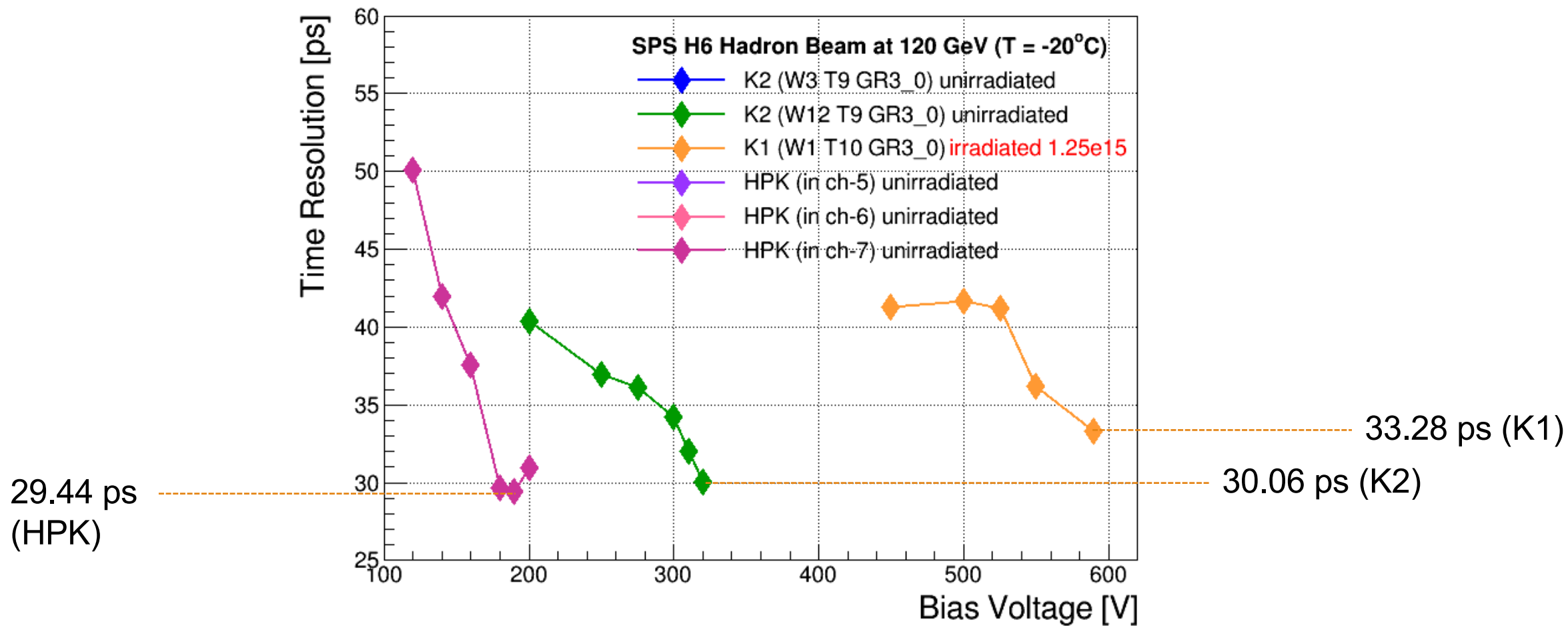
Collected Charge vs Bias Voltage using CERN test beam



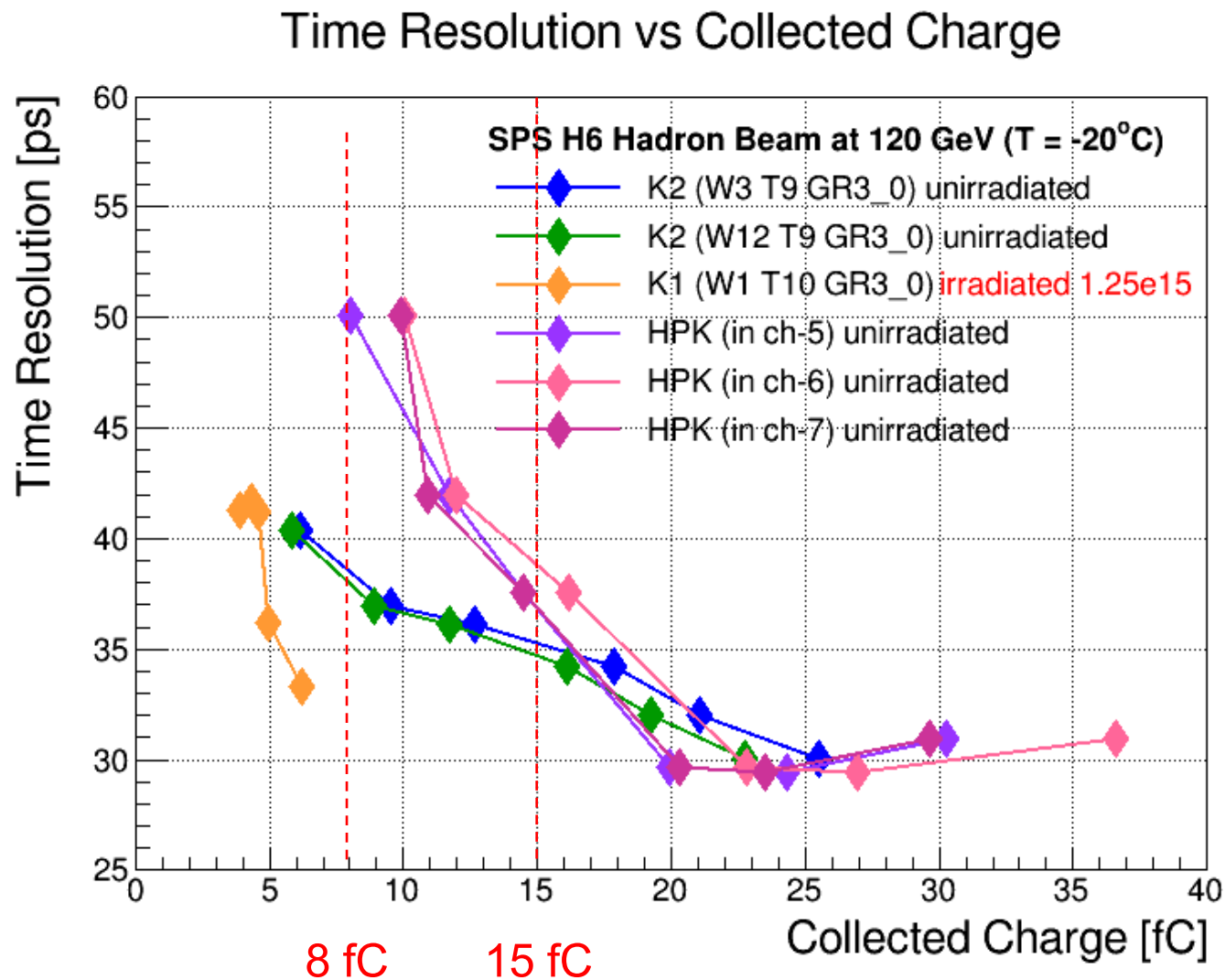
Characterization of the FBK-LGAD devices
manufactured at an external foundry for
large-volume productions, Leonardo Lanteri

Timing Resolution vs Bias Voltage using CERN test beam

Time Resolution vs Bias Voltage

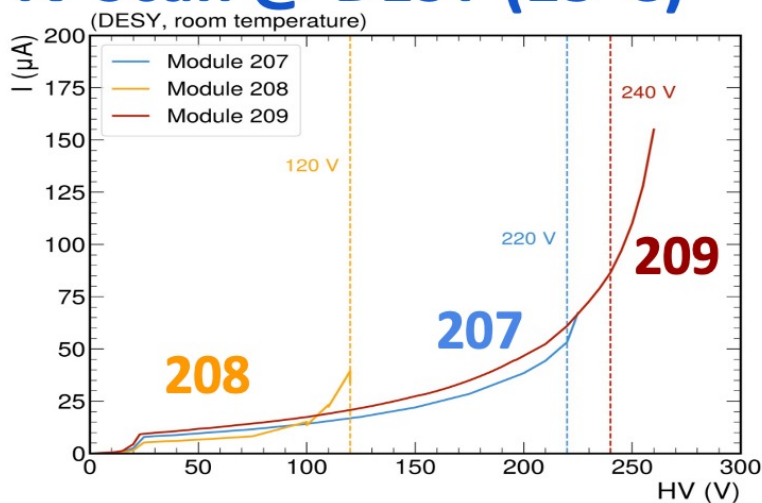


Timing Resolution vs Collected Charge using CERN test beam

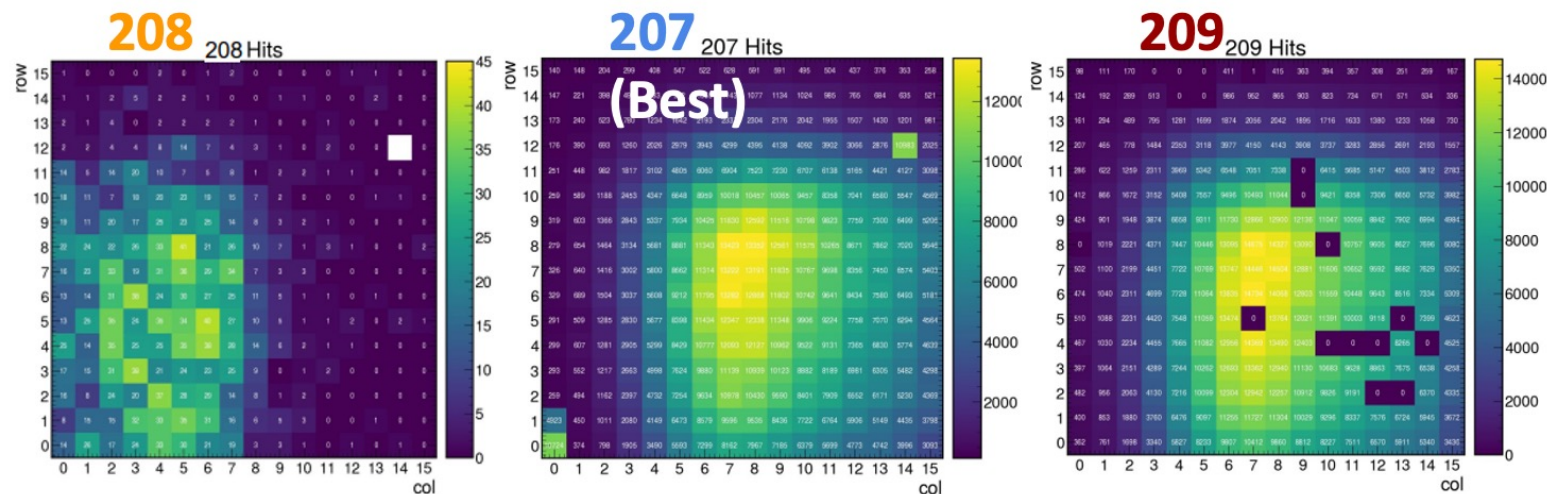


Test Beam @ DESY for bump-bonding quality test

IV Scan @ DESY (15°C)

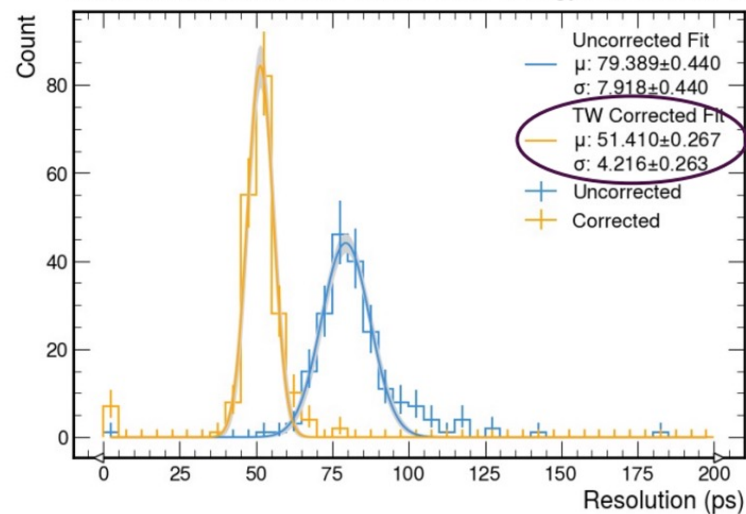


Hit map per hybrid (Bump-bonding quality)



Timing Resolution (Module 207)

Module: 207 Bias: 215.0 Offset: 20.0 Energy: 5.0 Power: i1



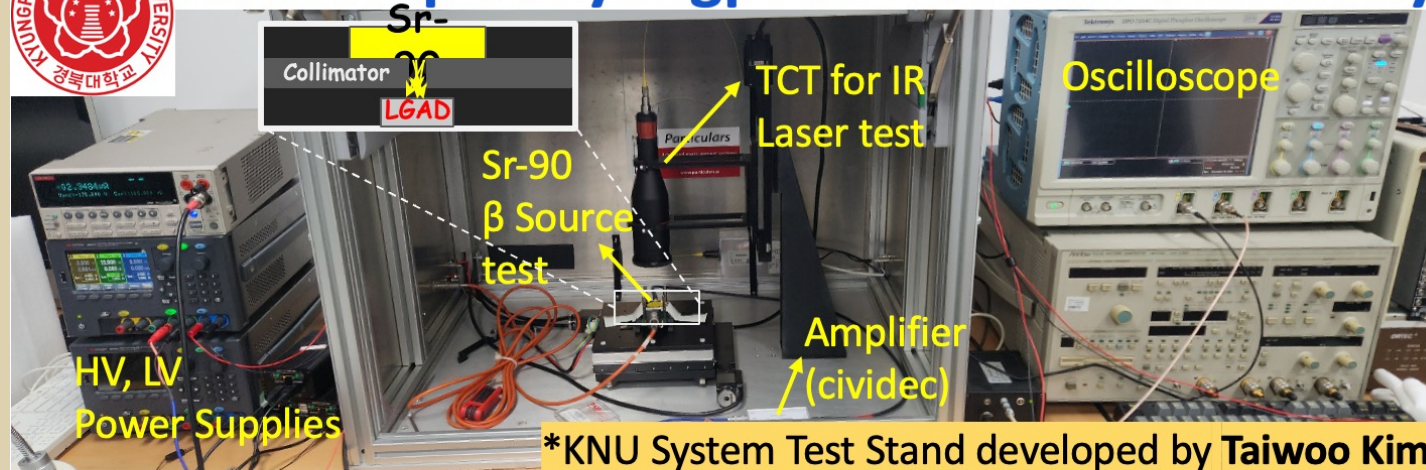
Highlights

- Collected >30 M events over 1 week (Single 207, 209 + Dual 207–208 modules)
- Stable DAQ up to 1.5kHz trigger rate $\Rightarrow$ Highest stat. ever in ETL system test!
- Good performance:
Solid Bump-bonding quality in 207, 209 (MICROSS)
Achieved 51-56 ps time resolution (after time walk correction) with 207, 209
- More interesting results will be updated!

Test Stand for ETL System Test at KNU



Test setup at Kyungpook National University



Status and Updates

- ✓ Update Laser setup to β source setup with Sr-90
- ✓ Performance test for UFSD K1-LGAD before IRRAD Test @KOMAC

IV Scan & Charge Collection (Pre-Irradiation baseline)

Done in 5x5 array using Laser and Sr-90 source with only-scope data (No ETROC data due to RB-FPGA IpGBT connection issue)

- ✓ Recently, the issue was resolved by updating "Clock config" in FPGA (Debugging & Verified at CERN Test Setup in B.904)

→ ETROC data integration (with hybrid module) : To be updated

Test Source Versatility @ KNU



IR Laser setup

Precise time calibration and charge collection measurement



β Source setup

Mimic minimum ionizing particle (MIP) response from Sr-90



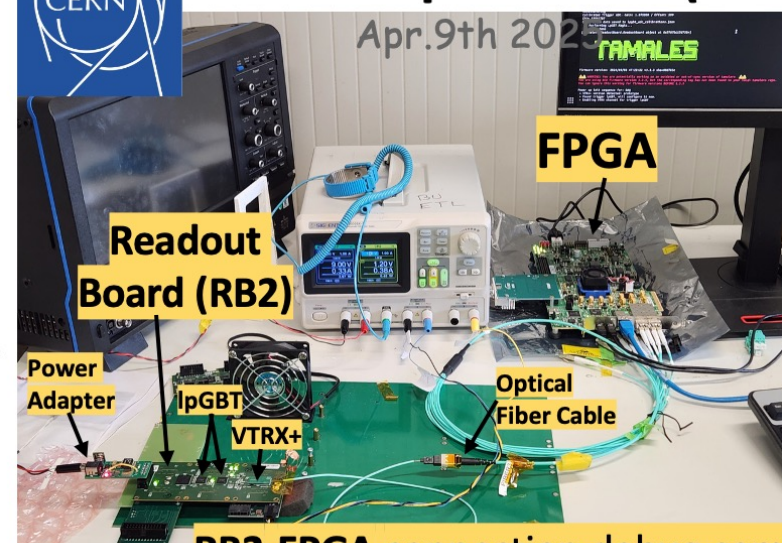
SOON

Next plan

full-size hybrid module testing, cosmic setup cooling test, etc ...



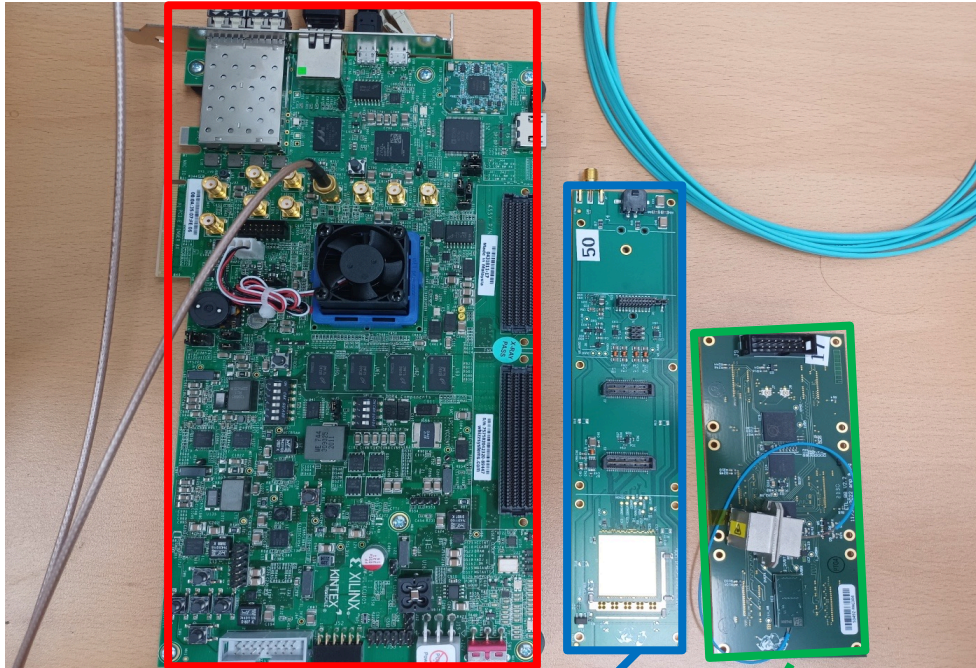
Test setup at CERN (Bld.904)



RB2-FPGA connection debug completed

MTD – Endcap Timing Layer (ETL) System Test at KNU

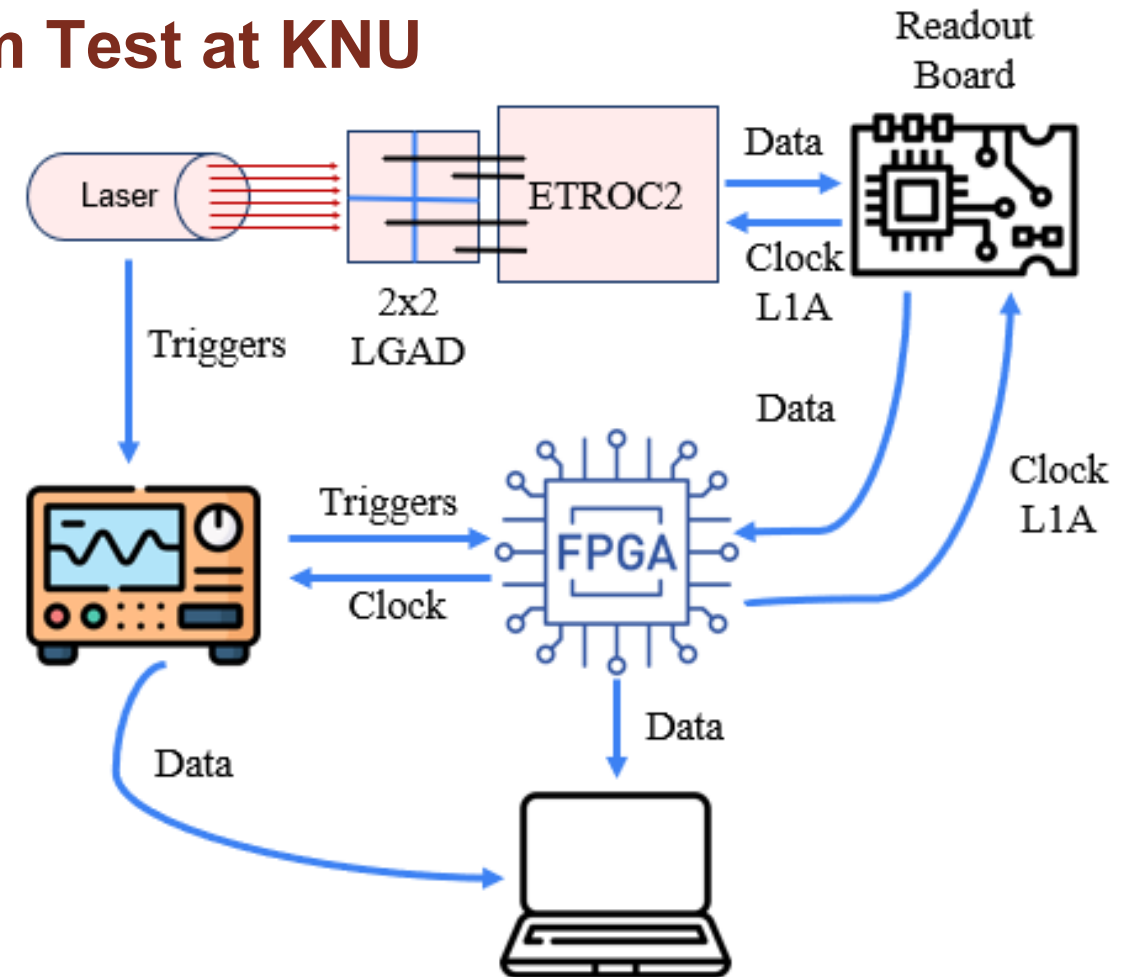
System Test Ingredient @ Korea



FPGA

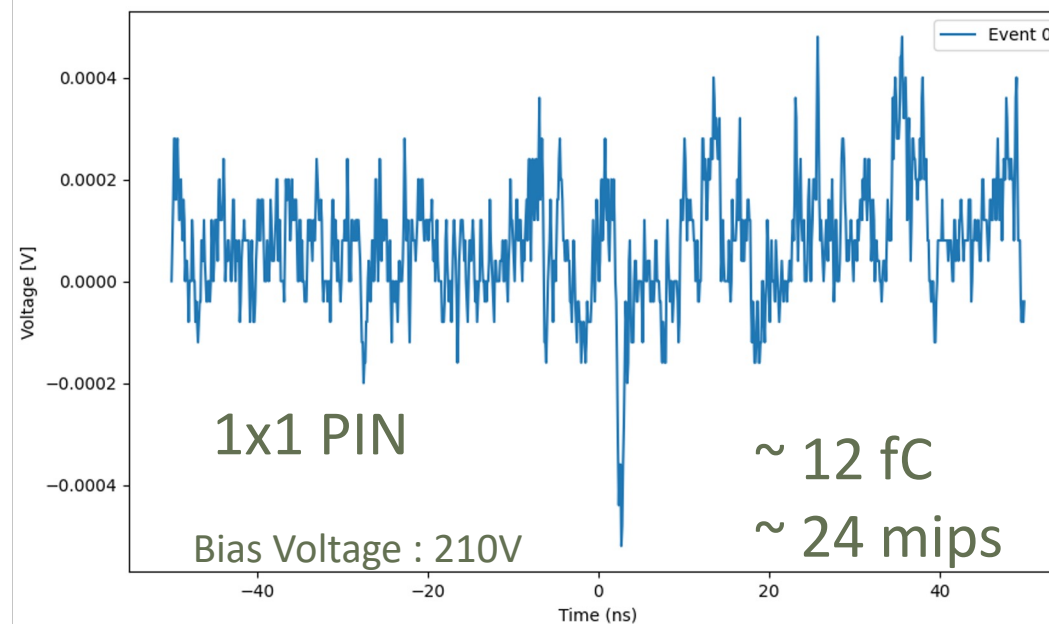
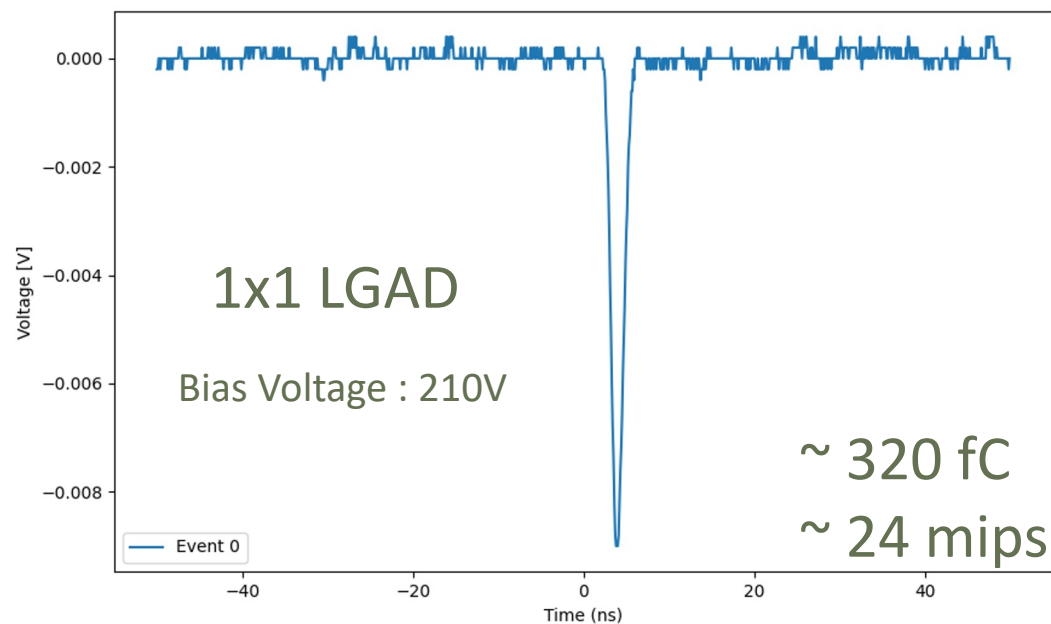
Module v0b

Readout Board v2.2



- System test stand for LGAD + ETROC system
- System test setup are constructed in Korea.
- Using this test stand, we can measure entire timing performance.
- We are planning to test with ETL Module v1 and v2 as well.

Pulse shape from LGAD using laser ($V_{\text{Bias}} = 210$)



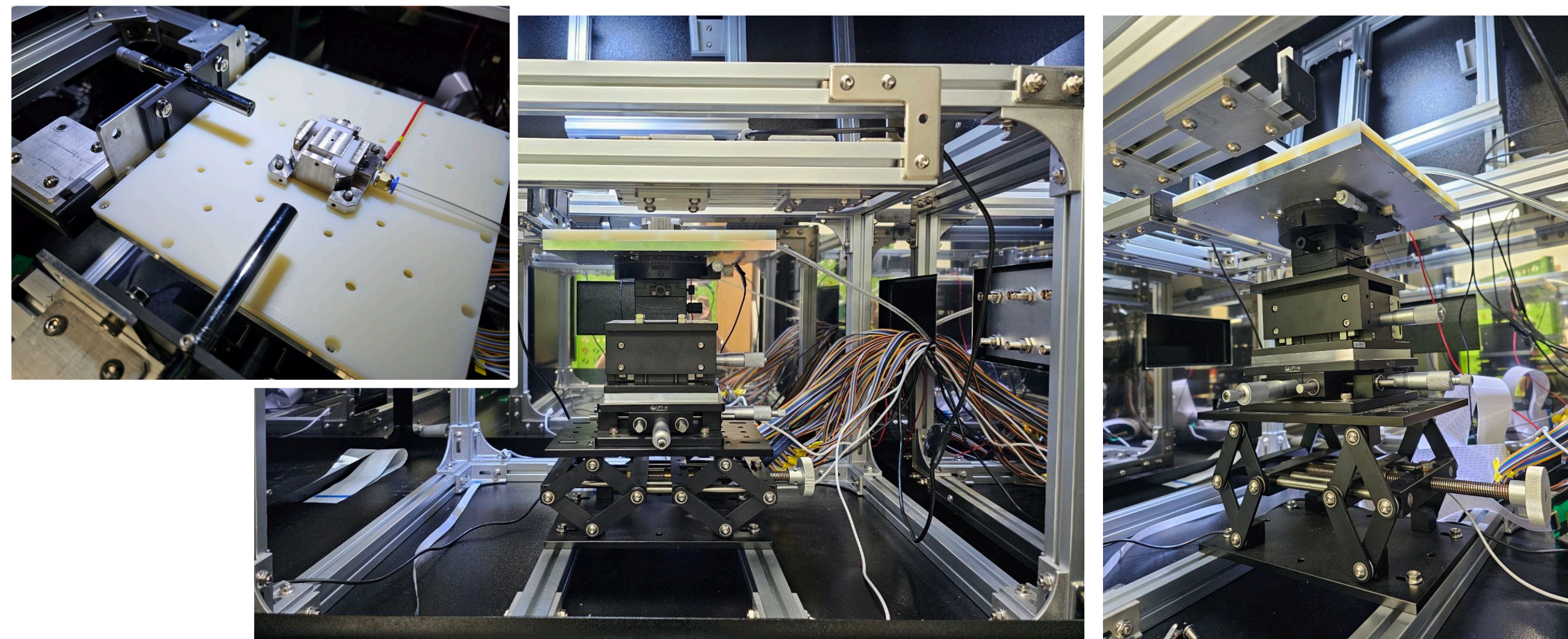
V_{Bias} measurement range:

- LGAD : 140 ~ 210 V
- PIN Diode : 160 ~ 210 V

Gain ~ a factor of 27
(1 mips ~ 0.5 fC)

- Laser Width : 81%
- DAC value : 2673 mV

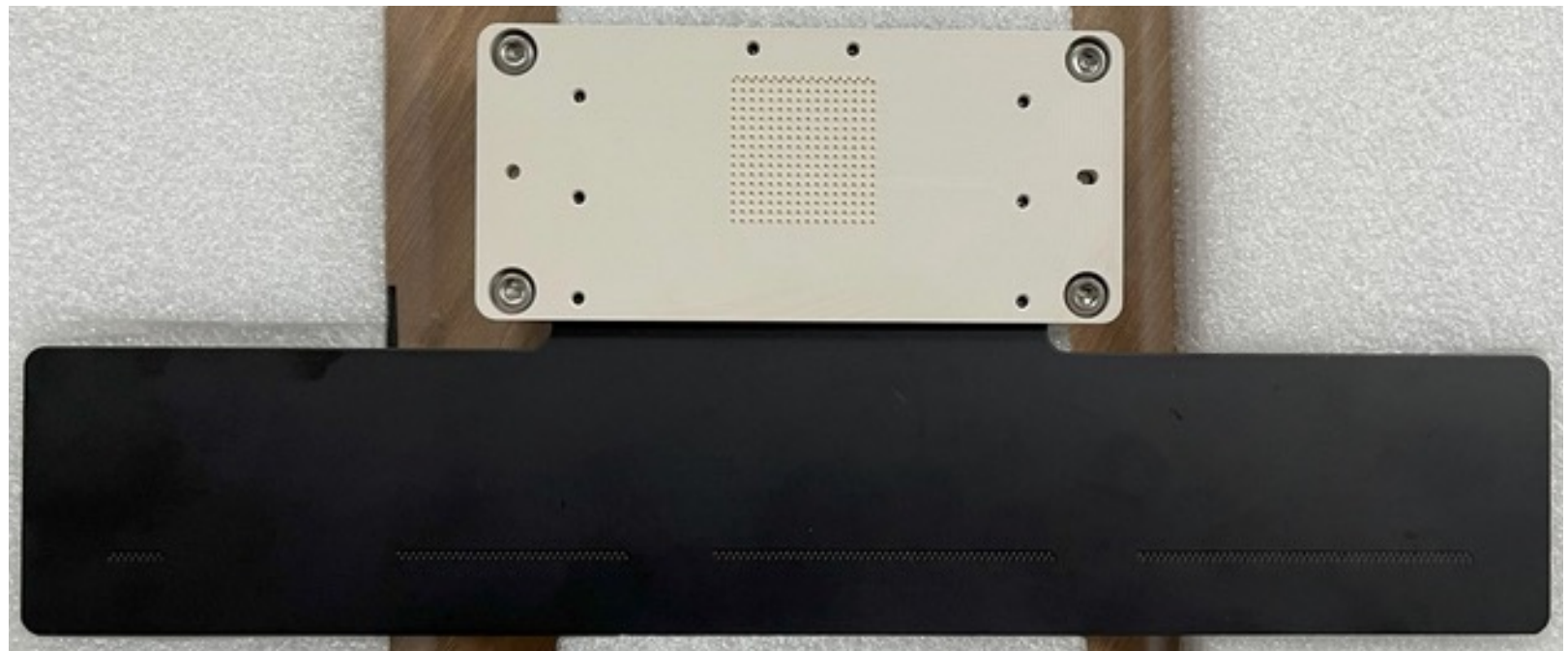
Development of probe card jig system test bench for LGAD QA/QC test



- Development of a probe card jig system integrated with a switching matrix
 - Manual probe card jig system to prepare a QA/QC test using an automated probe station

Probe card design

Front

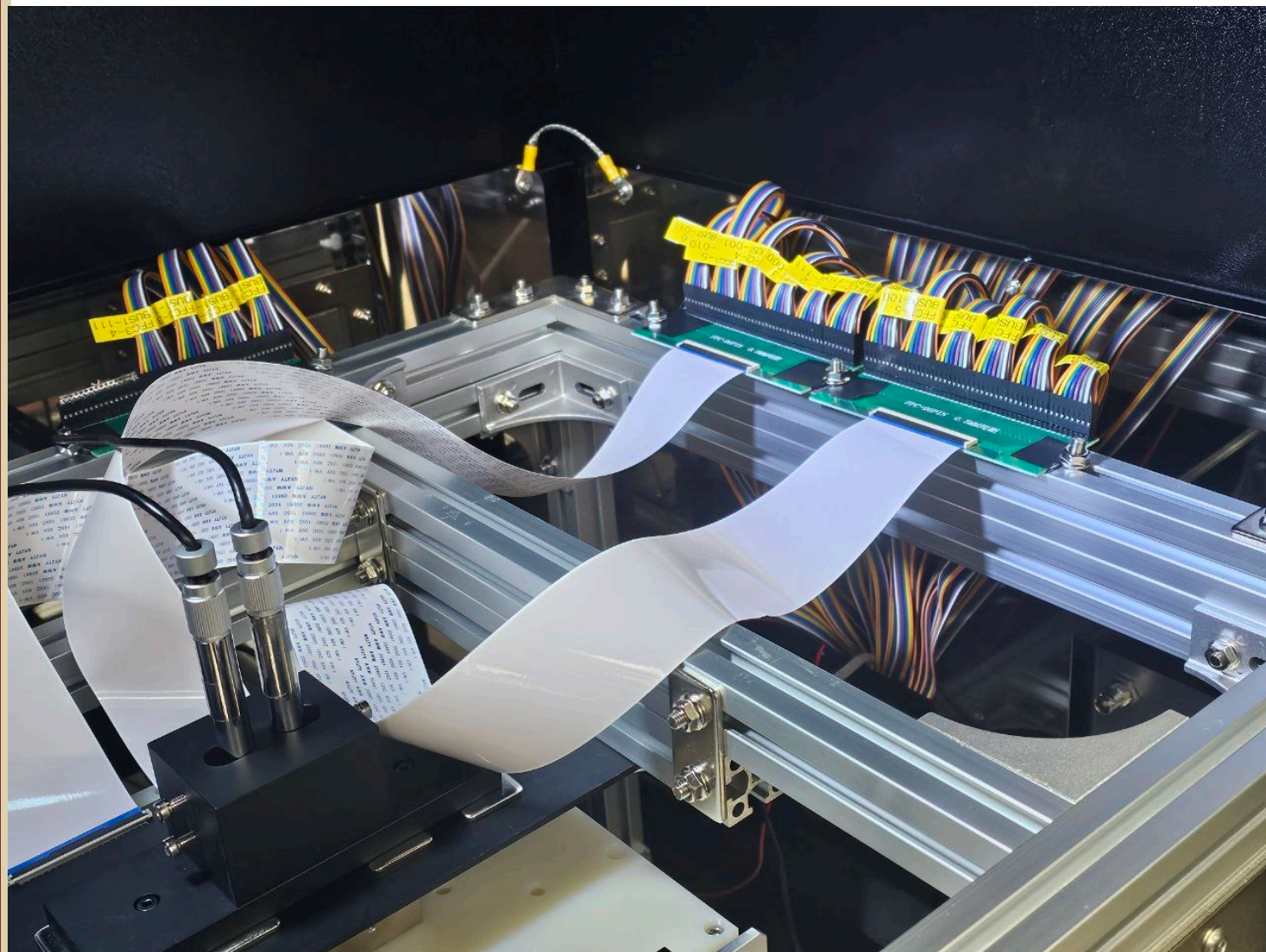


Back



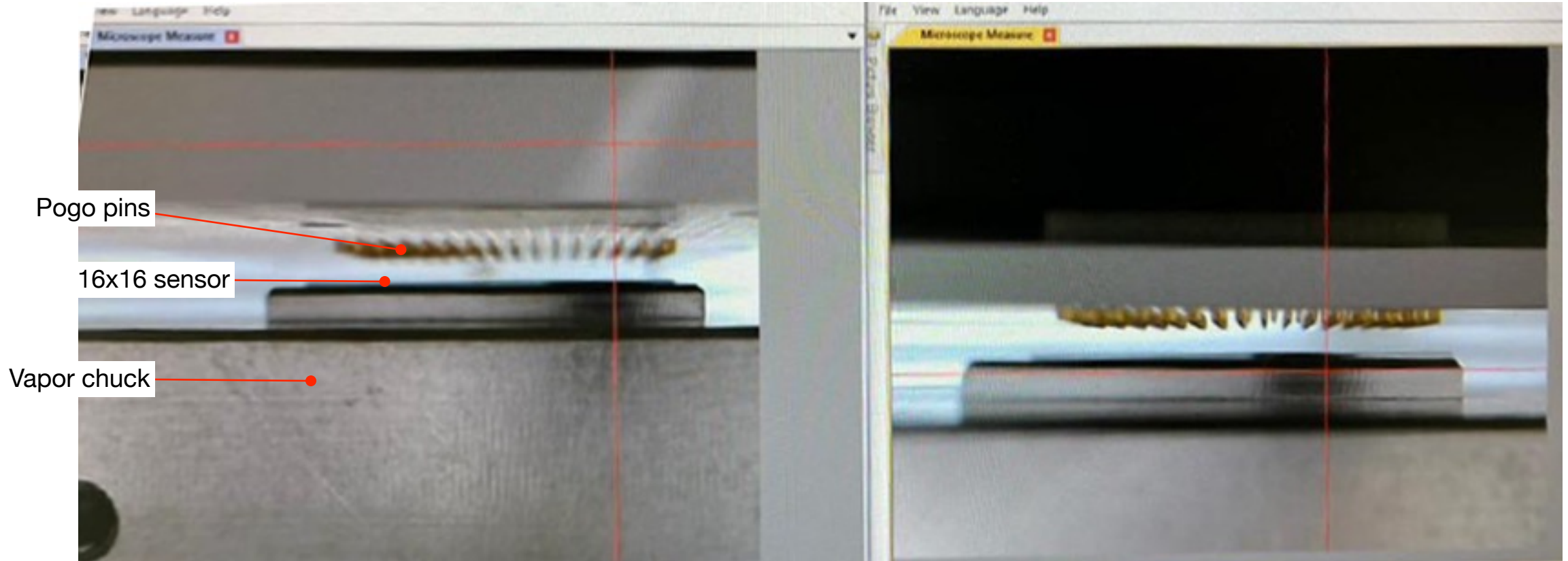
Readout cable
connectors

Probe Card 256 channel Switching Matrix System



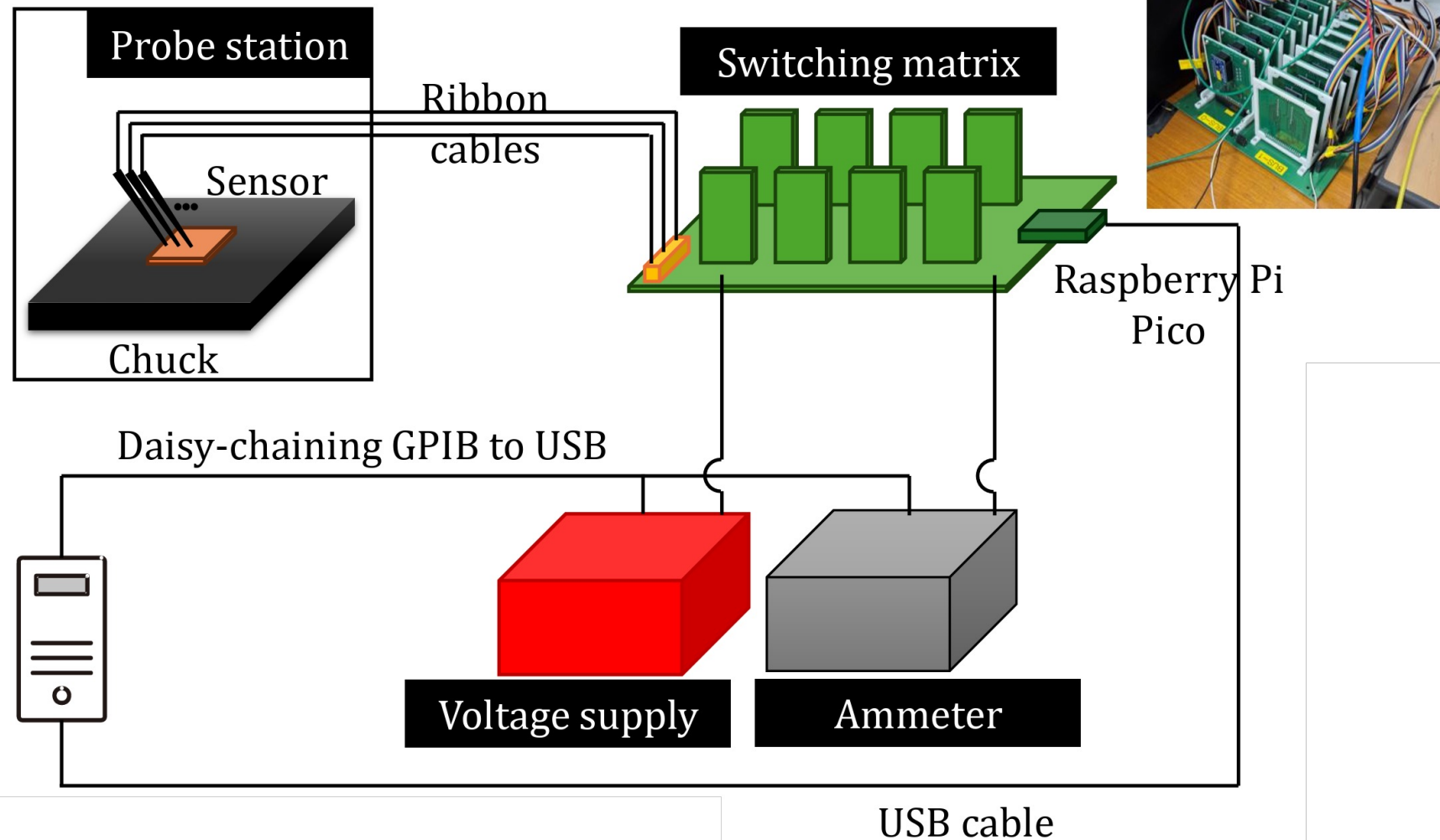
Pogo pins contact

Contact between sensor and pogo pins seen by two side usb cameras

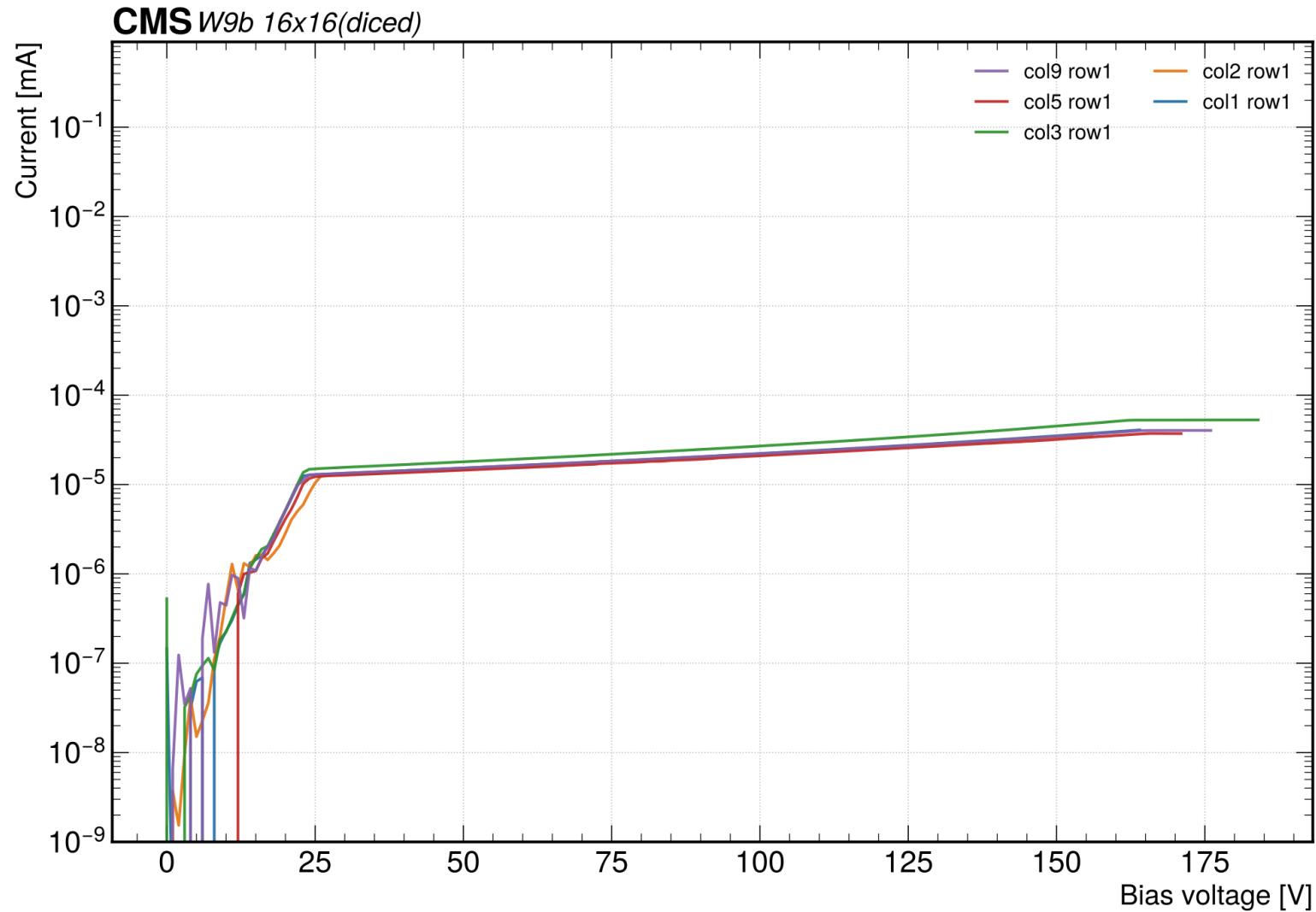


- Using two USB cameras, we adjust the tilt and the distance between the sensor and the probe card using the tilt and z stages.
- Checking good contact
 - Using a multimeter to confirm the connectivity between the two outermost BBs through the probe card.
 - If they are connected we assume the contact is good.

Probe card jig system DAQ workflow



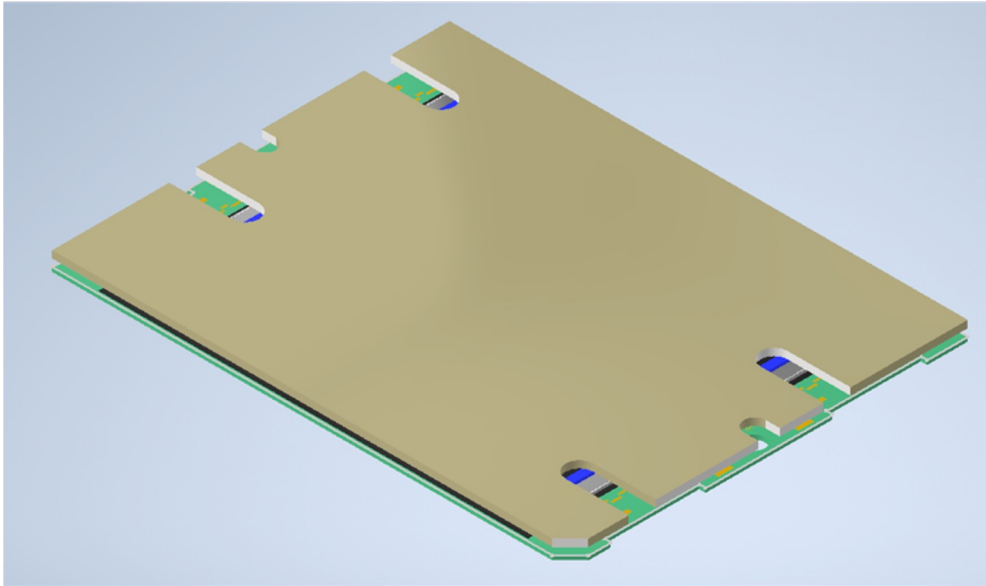
IV measurement results with the current jig system



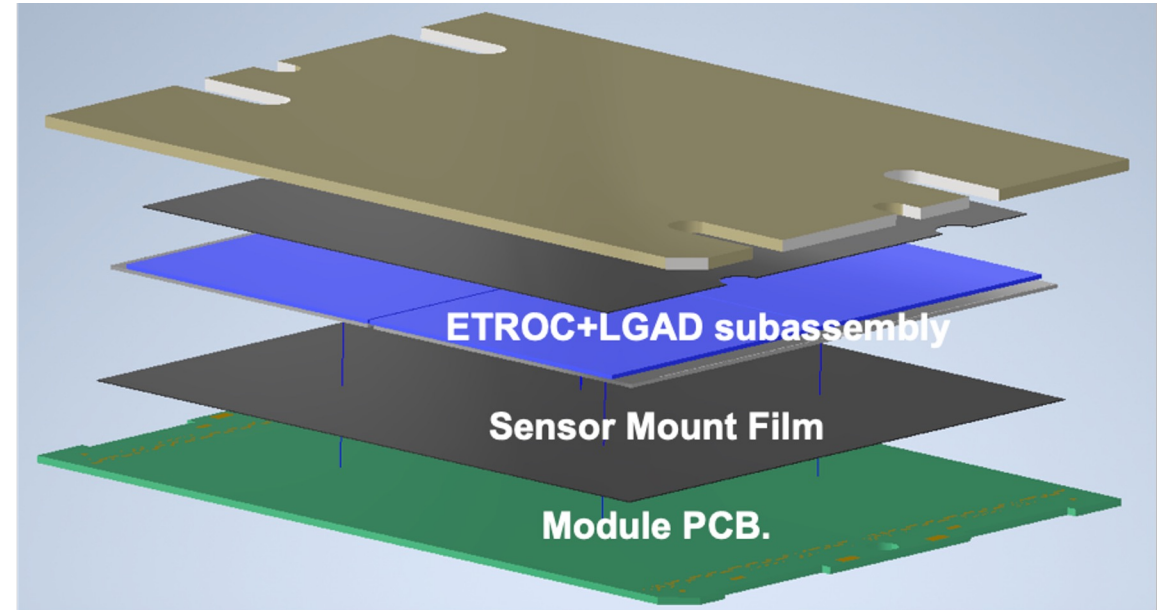
- Measured 5 different pads by manually changing the channels
- The IV curves look reasonable and are consistent each other

ETL Module design overview

❑ Module design overview



PCB + subassembly



Basic scheme of a module

❑ Module PCB

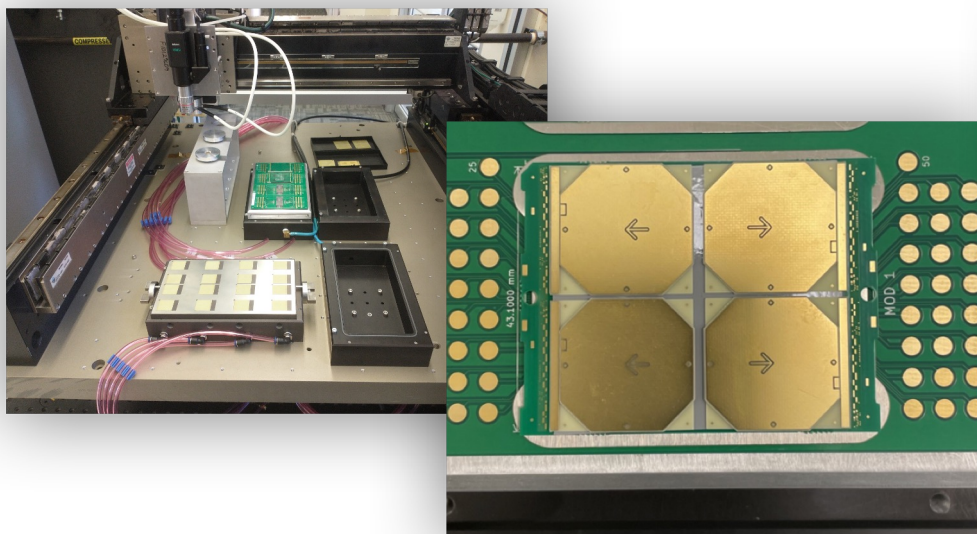
- Printed circuit board that serves as the power and readout interface for the module

❑ 4x ETROC+LGAD subassembly

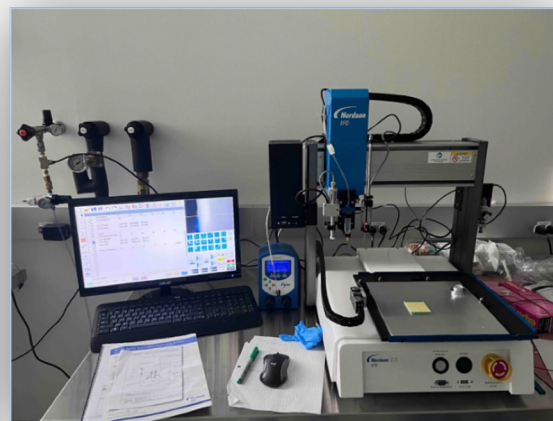
- 2x2 arrangement of bump-bonded assemblies
- Each of a 16x16 pixel LGAD sensor and an “ETROC” readout chip

Assembling the ETL Modules

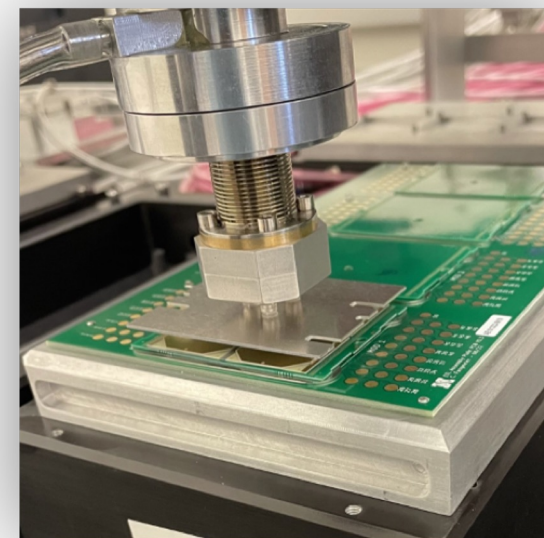
- ❑ The ETL detector will need ~8 thousand modules
- ❑ Each module will be made of 4 LGAD sensors and ETROCs
- ❑ An automated robotic gantry will be used for precision placement at the 10 micron level
- ❑ All modules will then be assembled into disks at CERN



Pick & place sensor +
PCB



Wirebond and
encapsulating

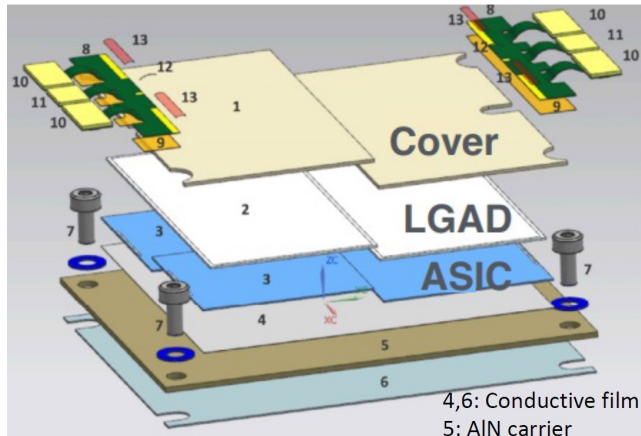


Apply film to baseplate, pick and
place, and cure film

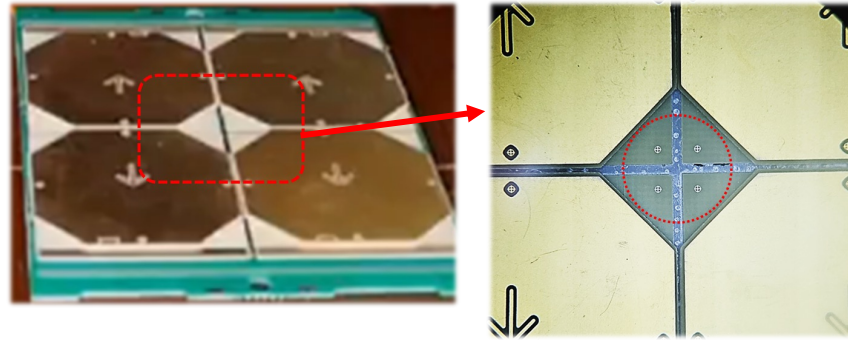
Module assembly test with dummy sample

- Module assembly pre-test for final product

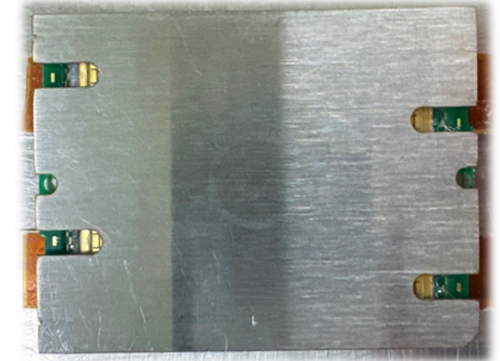
[Module assembly concept of LGAD sensor]



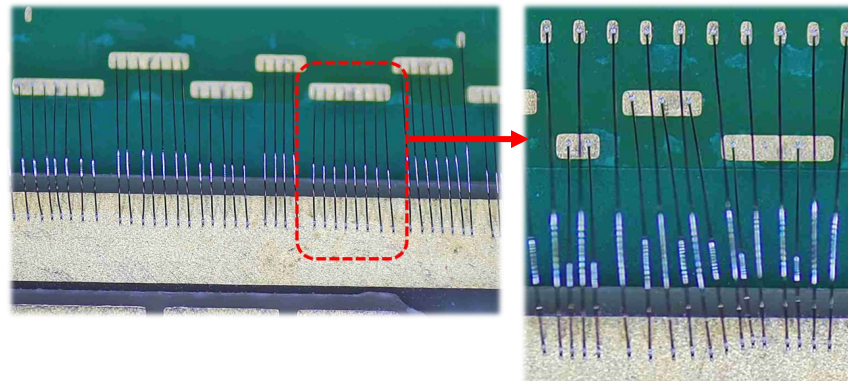
#1. Die attach of Bump bonded sample



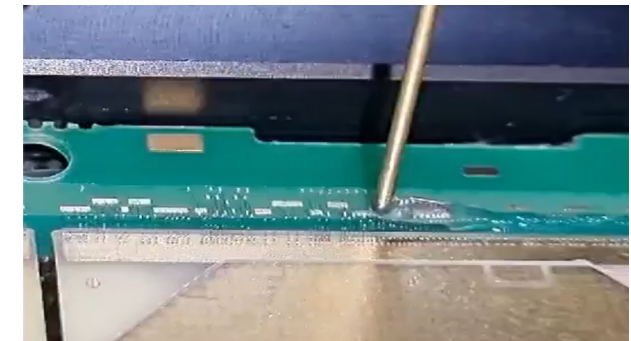
#4. Base plate covering



#2. Wire bonding to PCB board



#3. Wire passivation with glue

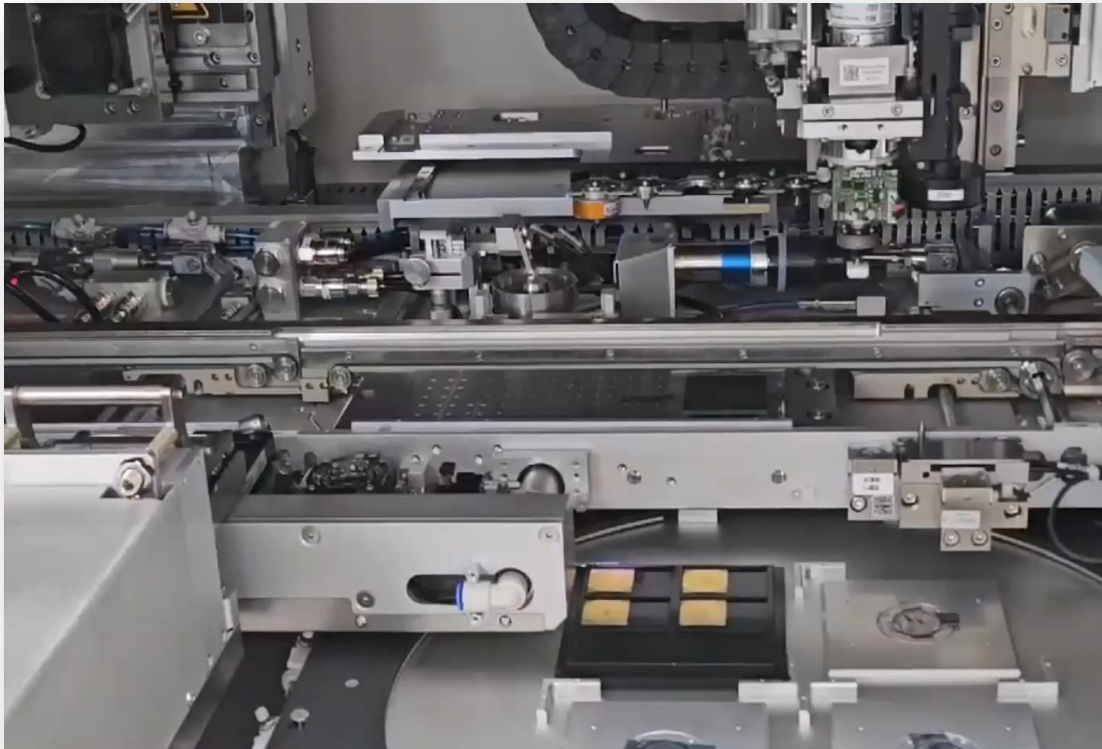




ETL Module Bonding

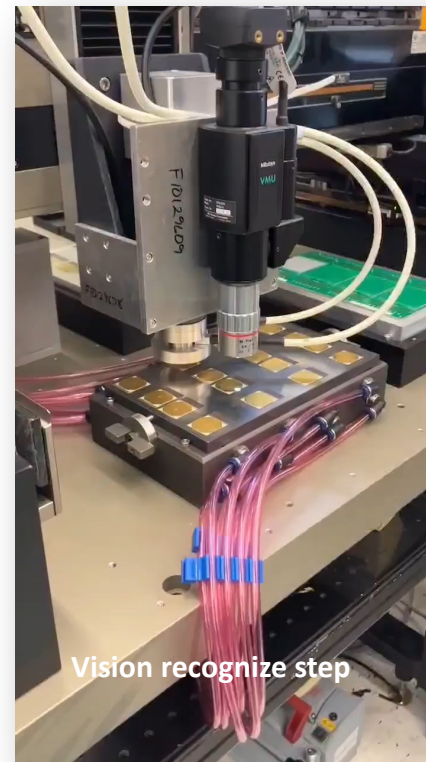
comparison

TOTAL WORKING TIME = 16sec / 1Chip



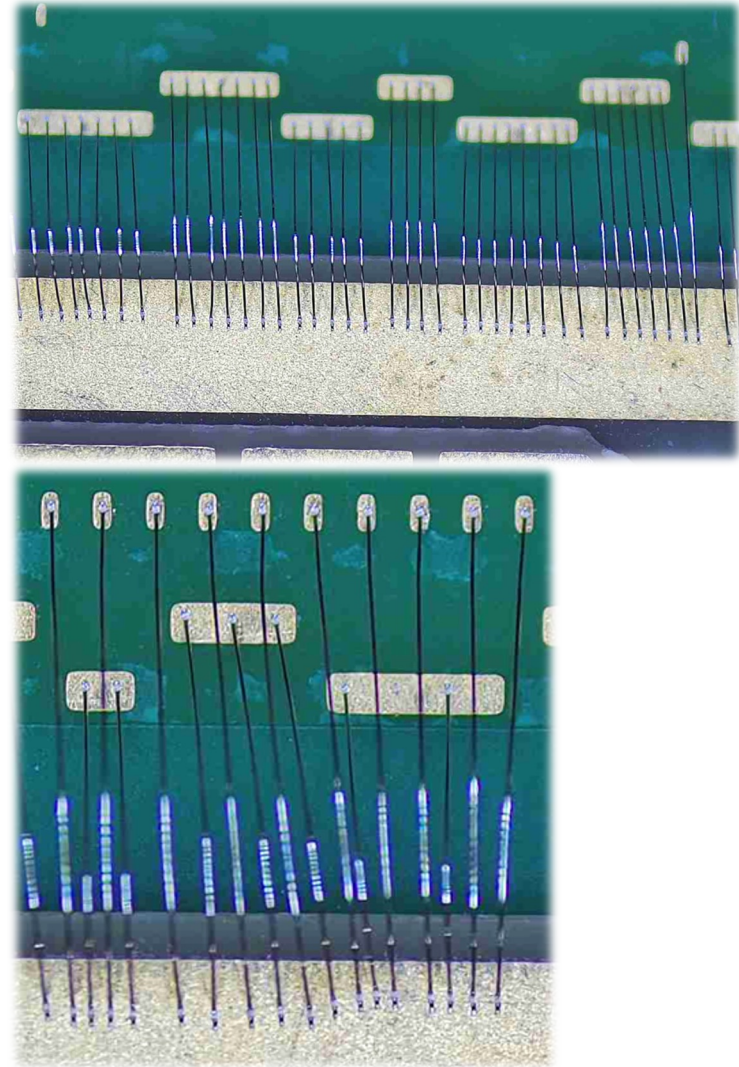
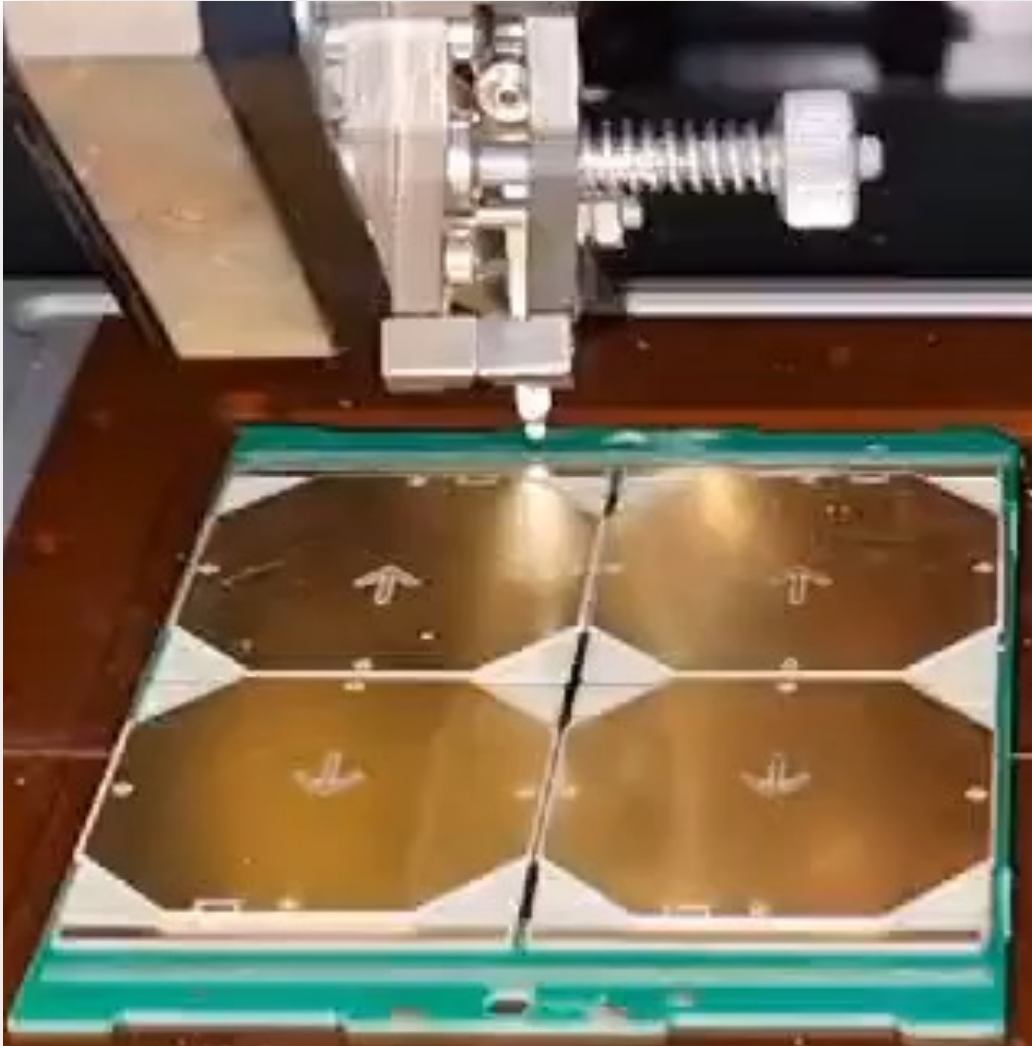
Korean vendor – die bonder machine

TOTAL WORKING TIME = 1min / 1Chip

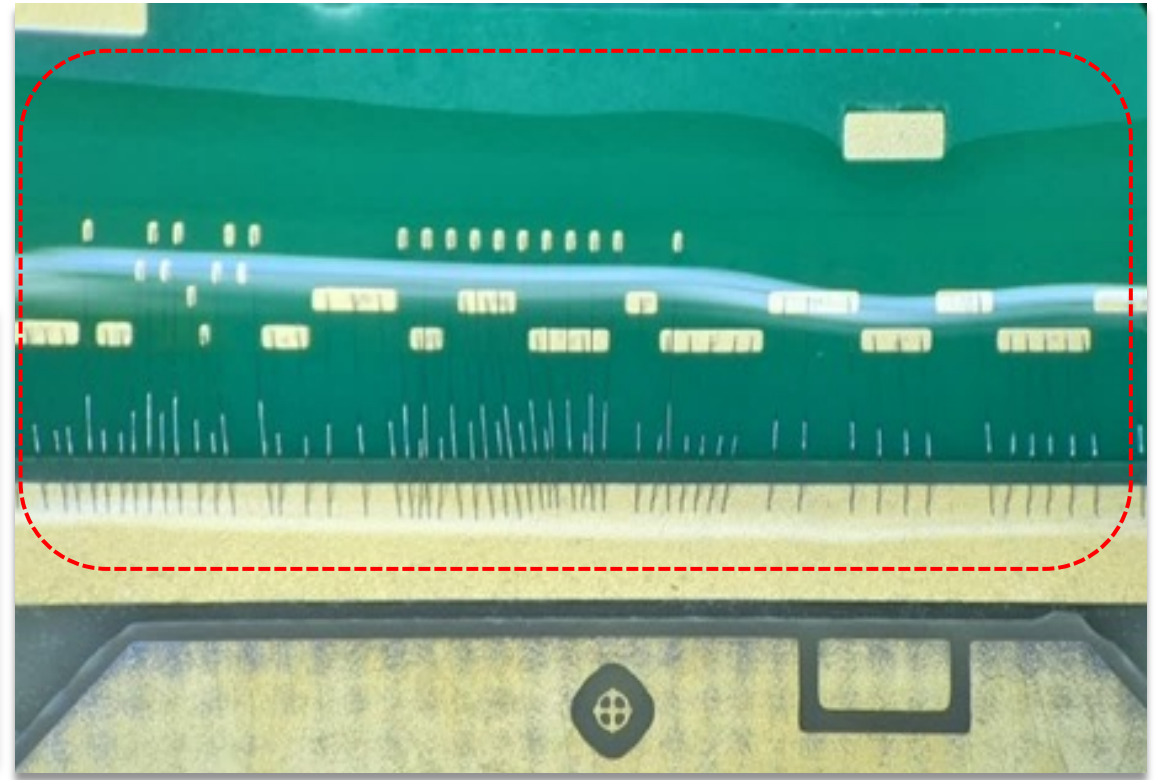
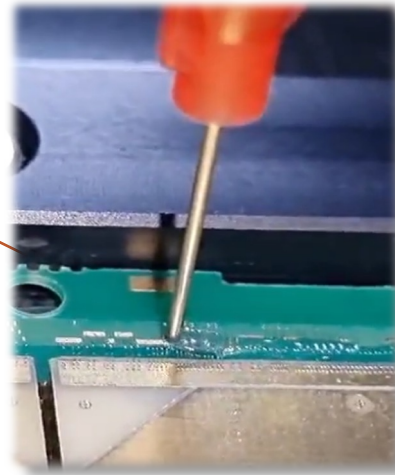


Fermilab – Gantry system

✓ ETL Module Wire Bonding

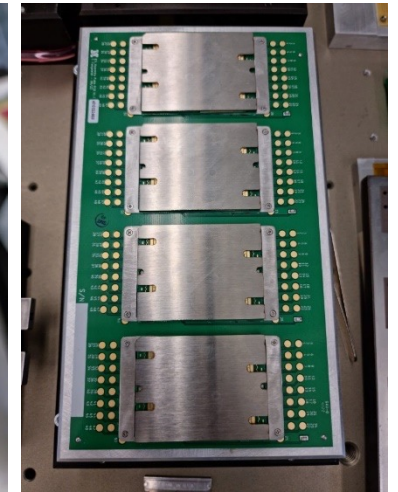
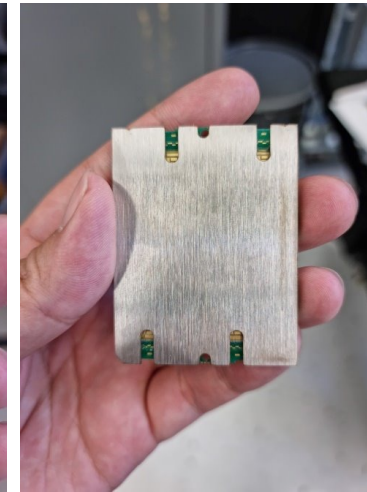
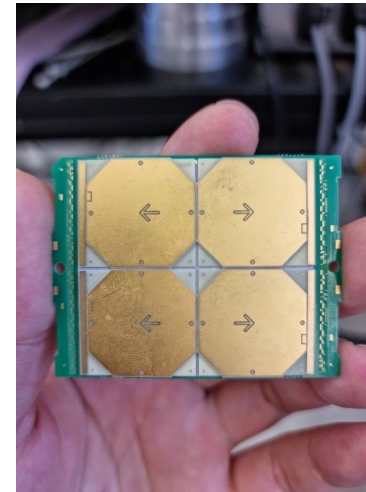
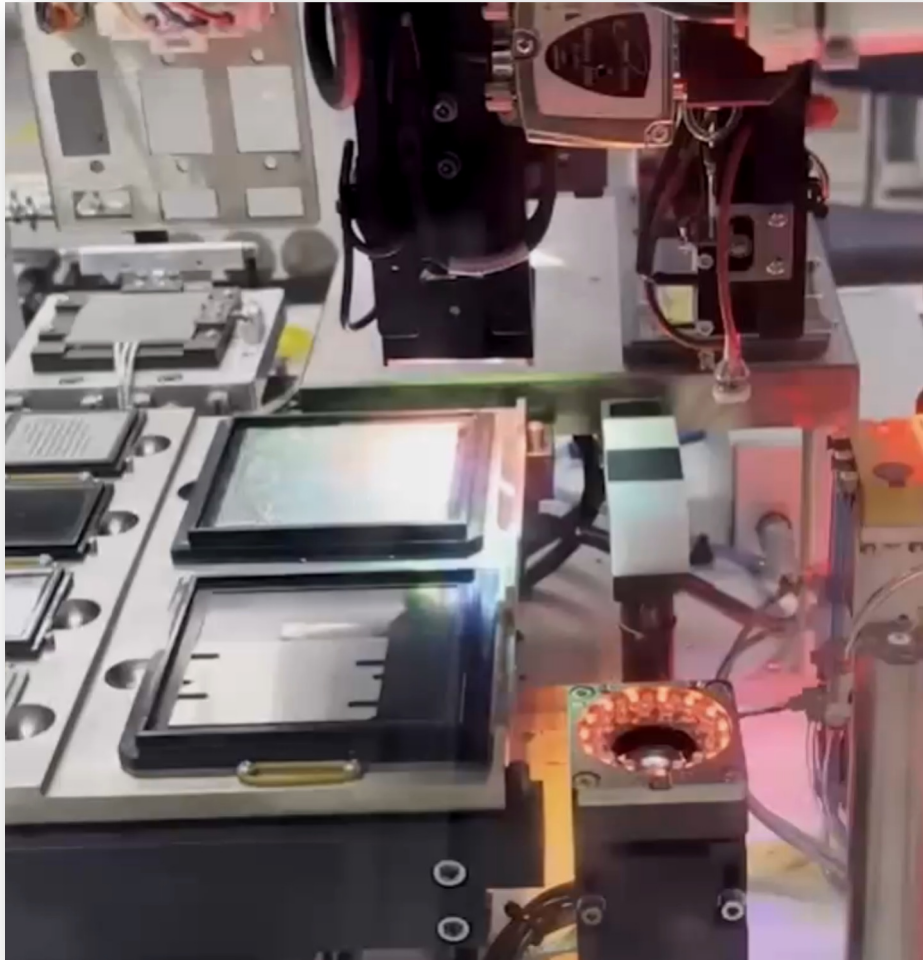


✓ ETL Module Encapsulation



MEMSPACK

✓ ETL Module Base Plate Bonding



- CERN Gantry system issue
 - Inaccurate position of baseplate
 - Unable to place automatically for current component condition
 - Bumpy surface of baseplate makes lift
 - Vacuum leakage issue

반도체 PACKAGING 장비

KCMS contribution for MIP Timing Detector (MTD)

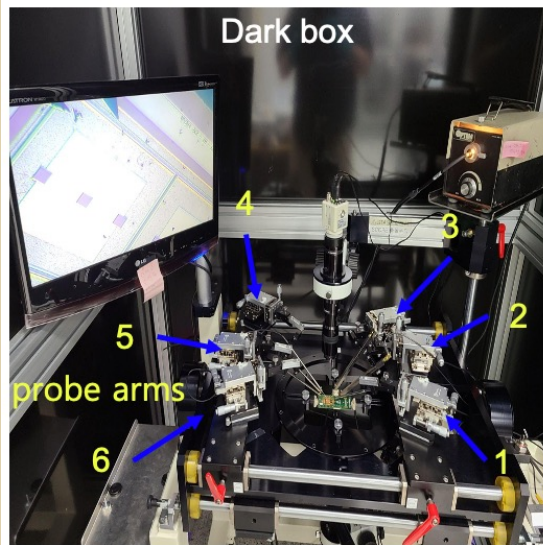
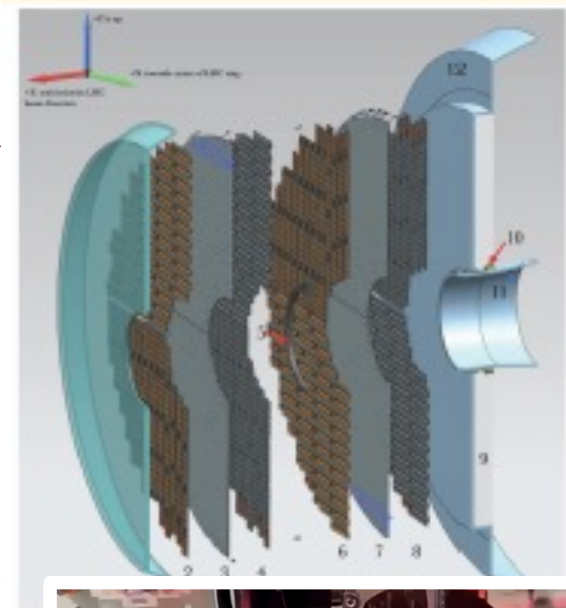
Mitigate the pileup effects at HL-LHC using precision timing information to enhance and expand the physics reach of our detector performance.

Main contributions from KCMS

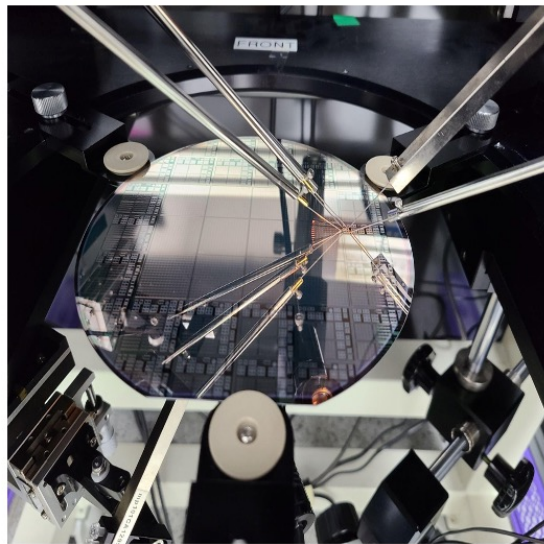
- Low Gain Avalanche Detector (LGAD) sensor development & production
- LGAD & ETROC Bump-Bonding development & processing
- ETL (Endcap Timing Layer) Module Assembly development & production

KCMS contribution for MTD : 2.2 MCHF (25% of the total endcap coverage)

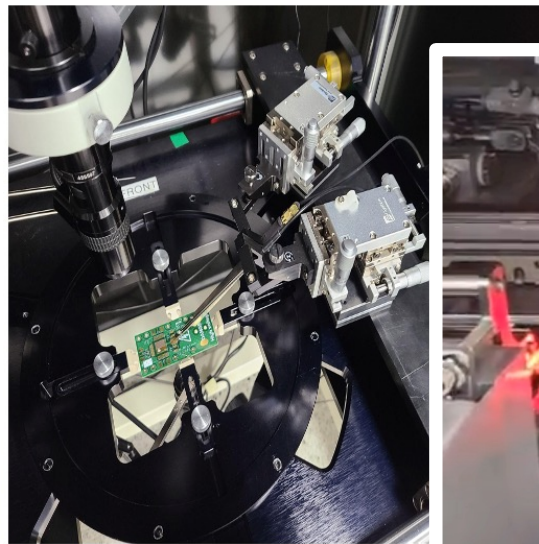
Total contribution with MTD on the Phase 2 will be ~6 MCHF



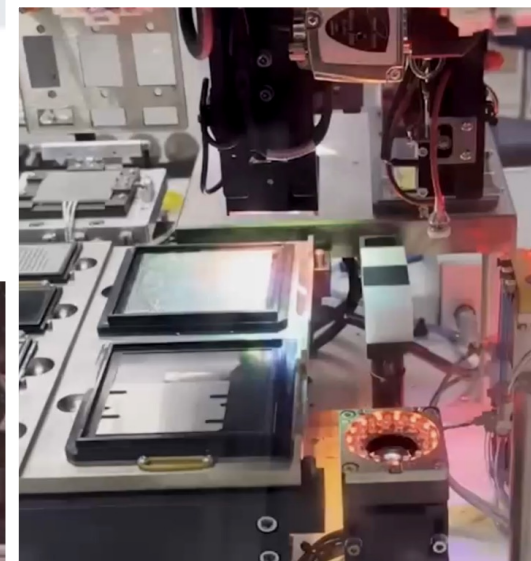
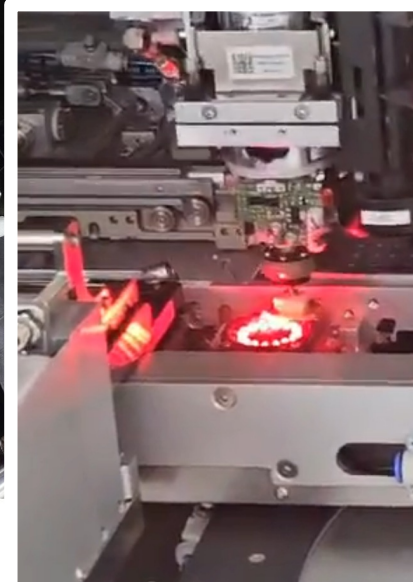
• Overview



• wafer tray



• sensor tray



Current Korea CMS Activities and Future plan

- ❑ Significant contributions to prototyping towards production
- ❑ LGADs prototyping and validation
 - Detailed testing of prototype LGADs informed vendor qualification
 - Probe station measurements to verify quality and uniformity of full-size wafers
 - Preparing the test bench setup with probe card and switching matrix
 - Participating various test beam at CERN and Fermilab
- ❑ System testing with LGAD+ETROC
 - Will receive 12-inch ETROC2 wafers from CERN
 - Active in System testing with LGAD+ETROC2, including test beam campaigns for validation of the performance of the LGADs +ETROC chain
- ❑ LGAD Wafer processing
 - Exploring wafer processing with one of the qualified LGADs vendors for wafer thinning, dicing, and surface preparation at Korean companies for the production phase
- ❑ Bump-bonding processing
 - Process testing with Korean vendors for LGAD-to-ETROC bump-bonding during production
- ❑ Module assembly
 - Korean vendor (Memspack) showed excellent performance for module assembly process with the die bonding machine.
 - Plan to irradiation test for encapsulation and glue using the KOMAC test beam October and December.





1st Korea CMS

MIP Timing Detector Workshop

일시: 2024.10.31.~11.02.

주최: 국립강릉원주대학교 첨단산업 인재양성 부트캠프 사업단



